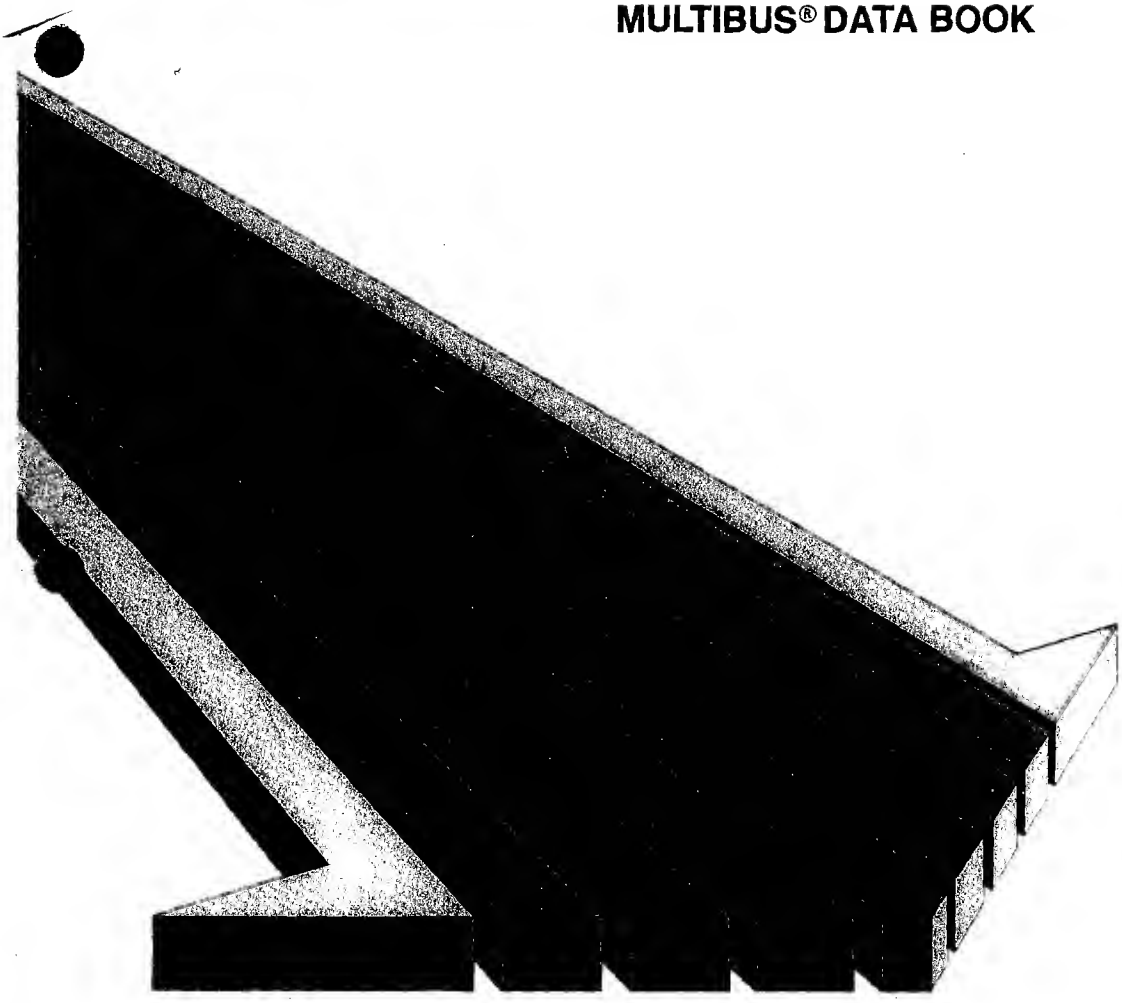
MULTIBUS® DATA BOOK



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intel

MULTIBUS® SYSTEM ARCHITECTURE: Its Origin and Evolution

The Beginning

MULTIBUS® system architecture is a relatively new phenomenon, but its roots can be traced back to the formative years of the microcomputer industry. Its history is one of humble beginnings and gradual, controlled evolution. An understanding of this history is useful in understanding the architecture.

In the early 1970's, the advent of VLSI component technology offered revolutionary benefits to the awaiting public. The emergence of these new "super chips" created opportunities and chaos in the marketplace, while competitive pressures forced companies to invest in the new concept. Everyone had to participate to be competitive, but not everyone had the design expertise.

Intel Corporation, being aware of the situation, introduced their Intellec™ series of development systems to provide design engineers with the software development tools needed to implement system designs. This software assist was welcomed, however customers also wanted to reduce the hardware design effort. Consequently, they purchased development system units, removed the boards for incorporation into their own boxes, and used the development system bus as the interface. They wanted the capability of designing their own custom boards, so a copy of the system bus specifications was requested. Intel then began distribution of the system bus specifications to the world.

Intel recognized the need for board level solutions, and pursued it. In 1976, they introduced their first board-level computer, the iSBC® 80/10, integrating a CPU, memory and I/O onto the first OEM single board computer. Soon after, the development system bus was given its own name, the MULTIBUS system bus, and the MULTIBUS architecture was born.

The new single board computers became an instant success, and an array of compatible products emerged from Intel and other vendors as well. Then in 1977-78, the microcomputer industry witnessed the introduction of new VLSI microcomputers. These new 16-bit machines had a new set of requirements. With a downward compatible evolution, the MULTIBUS structure supported these new processors, and reaffirmed the viability of the MULTIBUS system bus as a long-lived industry standard.

Standards Assure Success

Some of the characteristics which are required of a standard should be known before examining its advantages. The three most important requirements are:

- A standard must have industry acceptance and support.
- A standard must evolve to meet the needs of the future.
- A standard must have a single point of control.

In the case of the MULTIBUS system bus standard, it was introduced in 1976 and, in two years, had achieved wide spread industry acceptance. The bus had evolved to accommodate both 8- and 16-bit machines and their requirements. At first, Intel maintained control of the bus specifications, but now this task has been assumed by the IEEE. This single point of control ensures product compatibility between different board sources. MULTIBUS specifications were freely available to the industry and in the public domain. It was for these reasons that MULTIBUS architecture became the defacto industry standard, and also the IEEE bus standard, IEEE 796.

Advantages of Standards

The advantages that the MULTIBUS architecture standard offers to the user are based on growing support by multiple sources and continued evolution. The MULTIBUS market has shown phenominal growth in the number of MULTIBUS vendors. Another area of tremendous growth in the MULTIBUS market is in the number of MULTIBUS products made available to the industry by the growing MULTIBUS vendor base. Together, the MULTIBUS vendor and product growth trends reveal a healthy market.

A healthy open market offers tremendous benefits to potential users of MULTIBUS products. For instance, 120 MULTIBUS vendors means competition; and competition encourages competitive, low prices. The user pays less per MULTIBUS product which reduces overall system unit cost. Multiple sources of MULTIBUS products also means reduced risk to the user by eliminating the threat of sole source supply of important parts. Also, an open market which offers over 1000 MULTIBUS products provides a user with a wider range of choices. This selection of system solutions offers system designers almost unlimited flexibility and freedom. These pre-tested, off-the-shelf units mean a user can get to market quicker, with lower costs, and yet have the latest in VLSI technology. Additionally, a MULTIBUS user can optimize his

own resources and expertise, by concentrating on what he does best, and designing his own proprietary boards to the MULTIBUS standard. This allows the user to inject as much added-value into the system as he can in order to maximize his profit and be competitive. Only adherence to the MULTIBUS standard allows this flexible, added value concept to work.

In order to maintain adherence to a standard, the standard must continue to evolve to meet the need of the future. Since the MULTIBUS market needs are dynamic, the standard cannot remain static. It must be adaptable and upgradeable; continuing to evolve in a controlled deliberate manner.

Evolving Architecture: MULTIBUS®, iLBX™, iSBX™, MULTICHANNEL™

The MULTIBUS standard actually evolved in two different aspects: structure and architecture. The structure evolved from 8-bit to 16-bit capability, and direct addressing expanded from 64 KB to 16 MB. The architecture was expanded via the iLBX™ bus, iSBX™ bus, and MULTICHANNEL™ bus. These evolutionary expansions were necessary because a single system bus structure was no longer cepable of supporting the demands of todays high-speed, high-performance VLSI microprocessor technology, and its increasingly complex configurations. A single bus structure also tended to limit the available products to one dimensional "solutions".

The MULTIBUS architectural extensions occurred in the evolutionary process, because of the potential advantages in improved performance and flexibility.

The iLBX bus was created to provide users an architectural solution that extends the high performance benefits of a processor's on-board local bus to off-board memory resources. By supporting large amounts of high performance memory, the iLBX structure maximizes the performance potential for today's high-speed microprocessors by eliminating their need to access memory resources solely over the system bus. Powerful iLBX system modules can be created using the iLBX bus to connect a single board computer and a maximum of four memory cards. Acting as "virtual" iSBCs, these modules can directly access up to 16 megabytes of processor addressable memory over the iLBX bus and appear as though it were resident on the processor board. The iLBX bus preserves the advantages in performance and architecture of on-board memory, while allowing a wide range of memory capabilities to match application requirements.

The iSBX bus was created to provide users with a low cost, on-board expansion solution for MULTIBUS single board computers. Currently, the iSBX boards allow users to add capability to a single board computer in the areas of parallel I/O, serial I/O, peripheral controllers, and high-speed math, without going to the expense of adding another full MULTIBUS board. The iSBX bus compatible boards enable users to buy exactly the capabilities they require for their MULTIBUS based systems, which keeps both system size and system cost at a minimum.

The MULTICHANNEL bus was created to provide users with a separate path for DMA I/O block transfers. The ability of new VLSI microprocessors to process data at very high rates necessitates the connection of numerous high-speed I/O devices to the system bus. The major problem with this approach is that the attachment of these burst-type peripherals can saturate a generel purpose bus and reduce the computing performance of the system. The MULTICHANNEL bus was designed to eliminate this problem by providing for high speed (8 MB/sec) block transfers of data over an 8-/16-bit wide data path between peripherals and single board computer resources.

Development Support

Technicel support has developed over time, and now offers a wide variety of development/debug tools, documentation, and training for users of MULTIBUS-based systems. These technical tools provide the means to design, debug and implement microcomputer software and hardware systems with minimal effort.

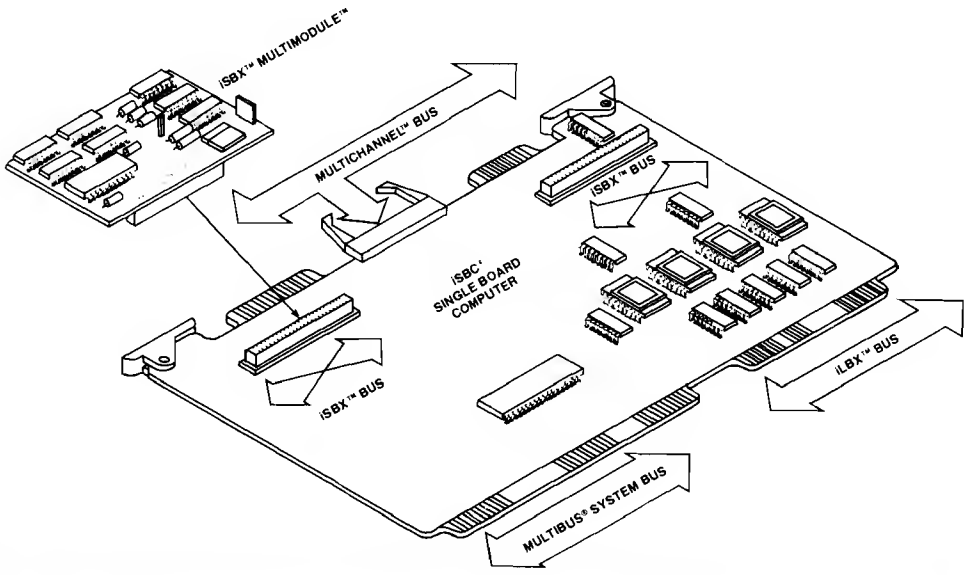
The Result

The continued evolution of the MULTIBUS standard, along with continued support and adherence by the market has made the MULTIBUS solution the fastest growing microcomputer system architecture in the board level marketplace. Its dominance of the 8-bit market and its growing influence in the 16-bit market is an example of its success as a true industry standard.

MULTIBUS® SYSTEM BUS

- IEEE 796 industry standard system bus
- Supports multiple processor systems with multi-master bus structure
- 8-bit and 16-bit devices share the same MULTIBUS® system resources
- Foundation of Intel's Total System Architecture: MULTIBUS,® iLBX,™ MULTICHANNEL™ and iSBX™ busses
- 16 Mbyte addressing capability
- Bus bandwidth of up to 10 megabytes per second
- Supported by a complete family of single board computers, memory, digital and analog I/O, peripheral controllers, graphics and speech recognition, packaging and software
- Supported by over 150 vendors providing over 1000 compatible products

The MULTIBUS® System bus is one of a family of standard bus structures resident within Intel's total system architecture. The MULTIBUS interface is a general purpose system bus structure containing all the necessary signal lines to allow various system components to interact with one another. This device interaction is built upon the master-slave concept. The "handshaking" between master and slave devices allows modules of different speeds to use the MULTIBUS interface and allows data rates of up to 5 million transfers per second. The MULTIBUS system bus can support multiple master devices (16) on a 18 inch backplane and can directly address up to 16 megabytes of memory. As a non-proprietary, standard system bus, the MULTIBUS interface has become the most prominent 8/16-bit microcomputer system bus in the industry with over 150 vendors supplying over 1000 MULTIBUS compatible products. Its success as the industry standard has been reinforced by adoption of the MULTIBUS specification by the Institute of Electrical and Electronic Engineers — (IEEE 796 System Backplane Bus). MULTIBUS-based systems have been designed into applications, such as, industrial automation and control, office systems and word processing, graphics systems and CAD/CAM, telecommunications systems and distributed processing.



FUNCTIONAL DESCRIPTION

Architectural Overview

The MULTIBUS® system bus is the physical framework and the conceptual foundation of Intel's total system architecture. It is a general purpose system bus used in conjunction with the single board computer concept to provide a flexible mechanism for inter-module processing, control and communication. The MULTIBUS interface supports modular CPU, memory and I/O expansion in flexible, cost effective microcomputer system configurations. These configurations implement single board computers and expansion modules in a multiple processor approach to enhance system performance. This enhanced performance is achieved through partitioning of overall system functions into tasks that each of several processors can handle individually. When new system functions are added (peripherals) more processing power can be applied to handle them without impacting existing processor tasks.

Structural Features

The MULTIBUS interface is an asynchronous, multiprocessing system bus designed to perform 8-bit and 16-bit transfers between single board computers, memory and I/O expansion boards. Its interface structure consists of 24 address lines, 16 data lines, 12 control lines, 9 interrupt lines, and 6 bus exchange lines. These signal lines are implemented on single board computers and a mating backplane in the form of two edge connectors resident on 6.75" x 12.00" form factor PC boards. The primary 86-pin P1 connector contains all MULTIBUS signal lines except the four address extension lines. The auxiliary 60-pin P2 connector contains the four MULTIBUS address extension lines, and reserves the remaining 56 pins for implementing the iLBX™ Execution Bus into the MULTIBUS system architecture.

Bus Elements

The MULTIBUS system bus supports three device categories: 1) Master, 2) Slave, 3) Intelligent Slave.

A bus master device is any module which has the ability to control the bus. This ability is not limited to only one master device. The MULTIBUS interface is capable of supporting multiple masters on the same system through bus exchange logic. Once access has been acquired by a master device, it has a period of exclusive control to affect data transfers through a generation of command signals, address signals and memory or I/O addresses.

A bus slave device is a module that decodes the address lines on the MULTIBUS and acts upon the command signals from the bus masters. Slave devices are not capable of controlling the MULTIBUS interface.

The intelligent slave has the same bus interface attributes as the slave device but also incorporates an on-

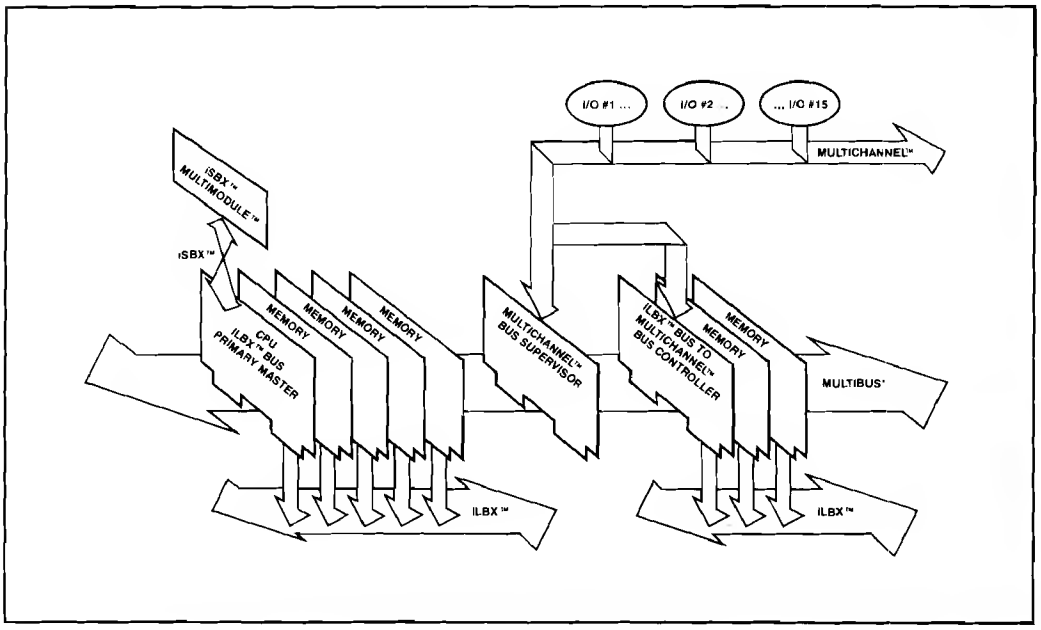


Figure 1. MULTIBUS® System Architecture

board microprocessor to control on-board memory and I/O tasks. This combination of on-board processor, memory and I/O allow the intelligent slave to complete on-board operations without MULTIBUS access.

Bus Interface/Signal Line Descriptions

The MULTIBUS system bus signal lines are grouped into five classes based on the functions they perform: 1) control lines, 2) address and inhibit lines, 3) data lines, 4) interrupt lines, 5) bus exchange lines. Figure 2 shows the implementation of these signal lines.

The MULTIBUS control lines are broken down into five sub-groups: clock signals (2), commands (4), acknowledge (1), initialize (1), and lock (1). The two clock signals provide for the generation of a master clock for the system and the synchronization of bus arbitration logic. The four command lines are the communications links between the bus masters and bus slaves, specifying types of operations to be performed such as reads or writes from memory or I/O. The transfer acknowledge line is the slave's acknowledgement that a requested action of the master is complete. The initialize signal is generated to reset the entire system to a known state. The lock signal is used by an active bus master to lock dual-ported for mutual exclusion.

The address and inhibit lines are made up of 24 address lines, two inhibit lines, and one byte control line. The 24 address lines are signal lines used to carry the address of the memory location or the I/O device that is being referenced. These 24 lines allow a maximum of 16 million bytes of memory to be accessed. When addressing an I/O device, sixteen address lines are used to address a maximum of 64 thousand devices. The two inhibit lines are used to allow different types of memory (RAM, ROM, etc.) having the same memory address to be accessed in a preferred priority arrangement. The byte control line is used to select the upper byte of a 16-bit word in systems incorporating 16-bit memory and I/O modules.

The MULTIBUS interface supports sixteen bi-directional data lines to transmit or receive information to or from a memory location or an I/O port.

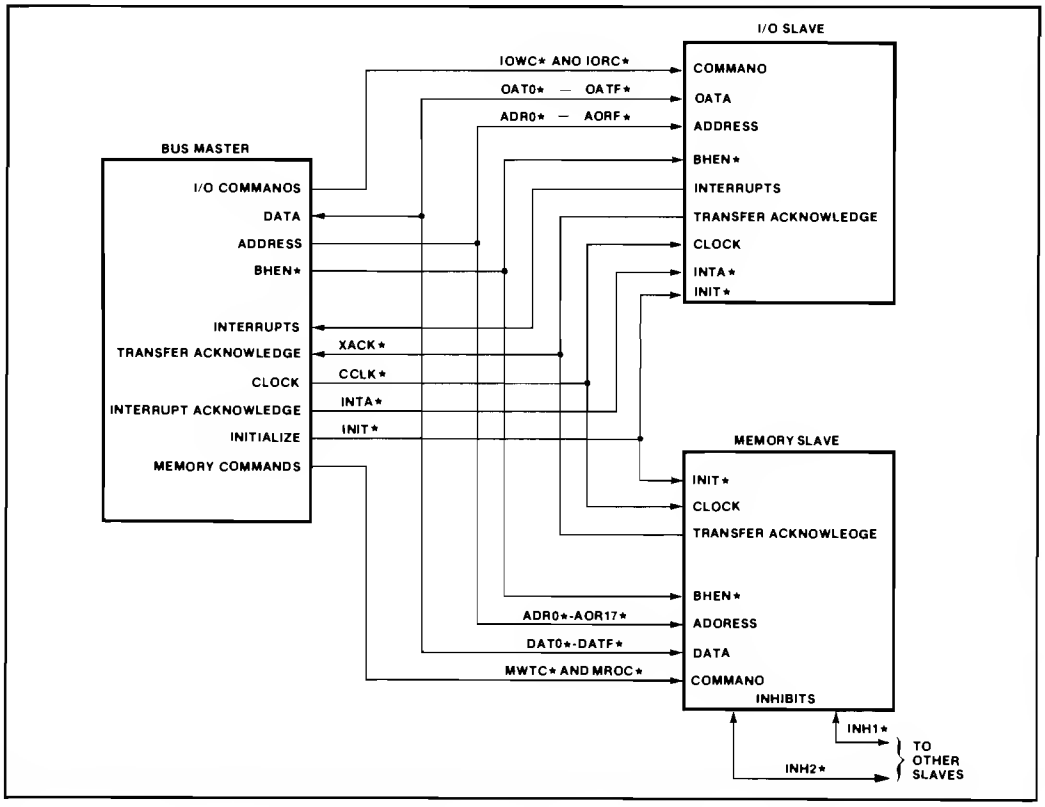


Figure 2. MULTIBUS® Interface Signal Lines

The MULTIBUS interrupt lines consist of eight interrupt request lines and one interrupt acknowledge line. Interrupts are requested by activating one of the eight interrupt request lines. The interrupt acknowledge signal is generated by the bus master when an interrupt request is received. It effectively freezes interrupt status and requests the placement of the interrupt vector address onto the data lines. There are six bus exchange lines that support two bus arbitration schemes on the MULTIBUS system bus. A bus master gains control of the bus through the manipulation of these signals. The bus request, bus priority, bus busy, and bus clock signals provide for a slot dependent priority scheme to resolve bus master contention on the MULTIBUS interface. Use of the common bus request signal line can save arbitration time by providing for a higher priority path to gain control of the system bus.

Bus Operation Protocol

DATA TRANSFER OPERATION

The data transfer operation of the MULTIBUS system bus is a straight-forward implementation of an asynchronous master-slave handshaking protocol. Figures 3 and 4 show the basic timing for a read and write data transfer operation. A MULTIBUS data transfer begins by having the bus master place the memory or I/O port address on the address bus. If the operation is a write, the data is also placed on the data lines at this time. The bus master then generates a command (I/O read or write, or memory read or write) which activates the appropriate bus slave. The slave accepts the data if it is a write operation, or places data on the data bus if it is a read. A transfer acknowledge is then sent to the bus master by the bus slave, allowing the bus master to complete its cycle, removing the command from the command line, and then removing the address and data from the MULTIBUS interface.

INTERRUPT OPERATIONS

The MULTIBUS interface supports two types of interrupt implementation schemes, Non-Bus Vectored and Bus Vectored. Non-Bus vectored interrupts are interrupts handled on the bus master which do not require the MULTIBUS interface for transfer of the interrupt vector address. The interrupt vector address is generated by the interrupt controller on the master and transfered to the processor over the local bus when an interrupt request line is activated by a slave module over the MULTIBUS interface. Bus vectored interrupts are interrupts which transfer the interrupt vector address along the MULTIBUS data lines from the slave to the bus master using the interrupt acknowledge command signal for synchronization. When an interrupt request occurs, the interrupt control logic on the bus master interrupts the processor, generating an interrupt acknowledge command that freezes the interrupt logic on the bus for priority resolution and locks the MULTIBUS system bus. After the bus master selects the highest priority active interrupt request lines, a set of interrupt sequences allow the bus slave to put its interrupt vector address on the data lines. This address is used as a pointer to interrupt the service routine.

BUS EXCHANGE TECHNIQUES

The MULTIBUS system bus can accommodate several bus masters on the same system, each one taking control of the bus as it needs to affect data transfers. The bus masters request bus control through a bus exchange sequence.

The MULTIBUS interface provides for two bus exchange priority techniques: a serial technique and a parallel technique. In a serially arbitrated MULTIBUS system, requests for system bus access are ordered by priority on the basis of bus slot location. Each master on the bus notifies the next lower priority master when it needs to use the bus, and it monitors the bus request status of the next higher priority-master. Thus, the masters pass bus requests along from one to the next in a daisy chain fashion. The parallel bus arbitration technique resolves system bus master priorities using external hardware in the form of a priority resolution circuit. This parallel arbitration logic is included in many commercially available cardcages.

Mechanical Implementation

BUS PIN ASSIGNMENTS

Printed circuit boards (6.75″ x 12.00″) designed to interface to the MULTIBUS system bus have two connectors which plug into the bus backplane. These connectors, the 86-pin P1 (Primary) and the 60-pin P2 (Auxiliary), have specific pin/signal assignments. Because of this, the designer must insure that the MULTIBUS backplane being designed is compatible (pin-for-pin) with these two connectors. Tables 1 and 2 show the pin/signal assignments for the P1 and P2 edge connectors. The MULTIBUS interface connection is accomplished via a rigid backplane that has connectors that mate to the P1 (43/86-pin) board edge connector and allows for connectors that mate to the P2 (30/60-pin) board edge connector. Figure 5 shows a typical MULTIBUS backplane. Figure 6 displays the connector and pin numbering convention. Figure 7 shows the standard MULTIBUS form-factor printed wiring board outline.

Please refer to Intel's MULTIBUS specification and iLBX bus specification for more detailed information.

Table 1. MULTIBUS® Pin/Signal Assignment — (P1)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Pri. In	16	BPRO*	Bus Pri. Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Cmd	20	MWTC*	Mem Write Cmd
	21	IORC*	I/O Read Cmd	22	IOWC*	I/O Write Cmd
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (disable RAM)
Bus Controls and Address	25	LOCK*	Lock	26	INH2*	Inhibit 2 (disable PROM or ROM)
	27	BHEN*	Byte High Enable	28	AD10*	
	29	CBRQ*	Common Bus Request	30	AD11*	Address
	31	CCLK*	Constant Clk	32	AD12*	Bus
	33	INTA*	Intr Acknowledge	34	AD13*	
Interrupts	35	INT6*	Parallel	36	INT7*	Parallel
	37	INT4*	Interrupt	38	INT5*	Interrupt
	39	INT2*	Requests	40	INT3*	Requests
	41	INT0*		42	INT1*	
Address	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*	Address	48	ADRB*	Address
	49	ADR8*	Bus	50	ADR9*	Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
Data	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	Data	64	DATB*	Data
	65	DAT8*	Bus	66	DAT9*	Bus
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12Vdc	80	−12V	−12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

All Reserved pins are reserved for future use and should not be used if upwards compatibility is desired.

*Note: The Reserved MULTIBUS P2 connector pin/signal assignments are contained in Intel's iLBX Bus Specification.

Table 2. MULTIBUS® Pin/Signal Assignment — (P2)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
	1		Reserved	2		Reserved
	3		Reserved	4		Reserved
	5		Reserved	6		Reserved
	7		Reserved	8		Reserved
	9		Reserved	10		Reserved
	11		Reserved	12		Reserved
	13		Reserved	14		Reserved
	15		Reserved	16		Reserved
	17		Reserved	18		Reserved
	19		Reserved	20		Reserved
	21		Reserved	22		Reserved
	23		Reserved	24		Reserved
	25		Reserved	26		Reserved
	27		Reserved	28		Reserved
	29		Reserved	30		Reserved
	31		Reserved	32		Reserved
	33		Reserved	34		Reserved
	35		Reserved	36		Reserved
	37		Reserved	38		Reserved
	39		Reserved	40		Reserved
	41		Reserved	42		Reserved
	43		Reserved	44		Reserved
	45		Reserved	46		Reserved
	47		Reserved	48		Reserved
	49		Reserved	50		Reserved
	51		Reserved	52		Reserved
	53		Reserved	54		Reserved
Address	55	ADR16*	Address Bus	56	ADR17*	Address Bus
	57	ADR14*		58	ADR15*	
	59		Reserved, Bussed	60		Reserved, Bussed

All Reserved Pins are reserved for future use and should not be used if upwards compatibility is desired.

*Note. The Reserved MULTIBUS P2 connector pin/signal assignments are contained in Intel's iLBX Bus Specification.

SPECIFICATION

Word Size

Data — 8 and 16-bit

Memory Addressing

24-bits — 16 megabyte – direct access

I/O Addressing

16-bits — 64 Kbytes

Maximum Bus Backplane Length

18 inches

Bus Devices Supported

16 total devices — (Master, Slave, Intelligent Slave)

Bus Bandwidth

10 megabytes/sec — 16-bit

5 megabytes/sec — 8-bit

Bus Exchange Cycle

200 nsec – Best Case; 300 nsec – Worst Case (assuming no bus master is currently active on the bus.)

Electrical Characteristics

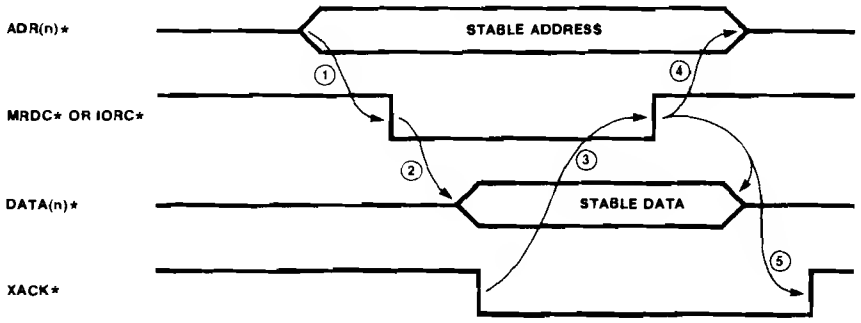
BUS POWER SUPPLY SPECIFICATIONS

Table 3.

	Standard[1]			
Parameter	Ground	+5	+12	−12
Mnemonic	GND	+5V	+12V	−12V
Bus Pins	P1-1,2,11,12, 75,76,85,86	P1-3,4,5,6, 81,82,83, 84	P1-7,8	P1-79,80
Tolerance	Ref.	±1%	±1%	±1%
Combined Line & Load Reg	Ref.	0.1%	0.1%	0.1%
Ripple (Peak to Peak)	Ref.	50 mV	50 mV	50 mV
Transient Response (50% Load Change)		100 μs	100 μs	100 μs

[1]Point of measurement is at connection point between motherboard and power supply. At any card edge connector a degradation of 2% maximum (e.g. voltage tolerance ±2%) is allowed.

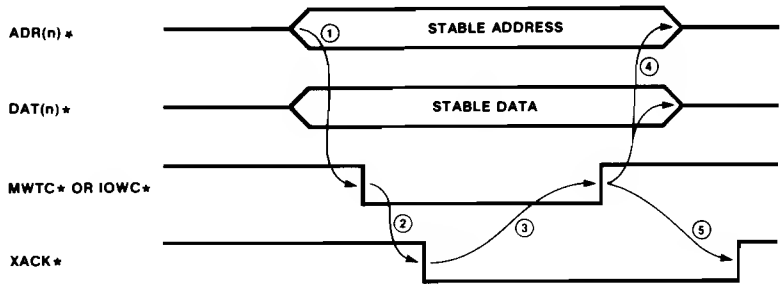
BUS TIMING



1. ADDRESS SETUP TIME: 50 NANOSECONDS MINIMUM.
2. TIME REQUIRED FOR SLAVE TO GET DATA ONTO BUS IN ACCORDANCE WITH SETUP TIME REQUIREMENT. XACK* CAN BE ASSERTED AS SOON AS DATA IS ON BUS.
3. TIME REQUIRED FOR MASTER TO REMOVE COMMAND.
4. ADDRESS AND DATA HOLD TIME; 50 NANOSECONDS MINIMUM.
5. XACK* AND DATA MUST BE REMOVEO FROM THE BUS A MAXIMUM OF 65 NANOSECONDS AFTER THE COMMAND IS REMOVED.

Figure 3. Memory or I/O Read Timing

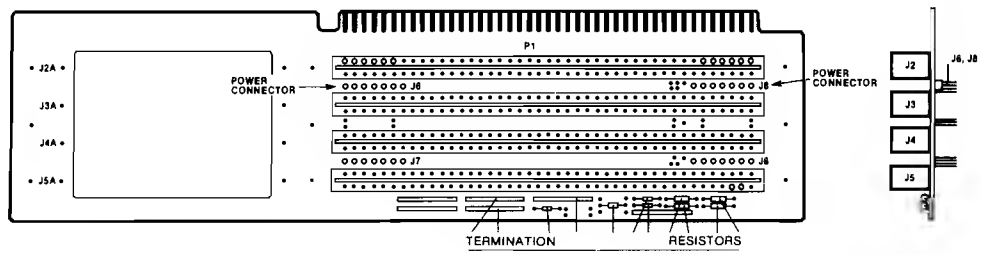
BUS TIMING (Con't)



1 ADDRESS AND DATA SETUP; 50 NANOSECONDS MINIMUM.
2 TIME REQUIRED FOR SLAVE TO ACCEPT DATA.
3 TIME REQUIRED FOR MASTER TO REMOVE COMMAND FROM BUS.
4 ADDRESS AND DATA HOLD TIME; 50 NANOSECONDS MINIMUM.
5 XACK* MUST BE OFF THE BUS 65 NANOSECONDS AFTER COMMAND.

Figure 4. Memory or I/O Write Timing

Physical Characteristics



PARTS LIST

1 PWB TERMINATION BACKPLANE
2 7 POST WAFER CONNECTORS (.156" PIN CENTERS) (J6 AND J6)
4 EDGE BOARD CONNECTORS, 43/86 PINS ON .156" CENTERS (J2-J5)
12 WIRE WRAP POSTS
4 10 PIN, 2.2K, 9 RES, 1.5W RESISTOR PACKS (RP1-RP4)
1 10 PIN, 1K, 9 RES, 1.5W RESISTOR PACK (RP5)
1 10 PIN, 1.1K, 9 RES, 1.5W RESISTOR PACK (RP6)
1 1K RESISTOR, 1/8W, ±5% (R1)
1 2.2K RESISTOR, 1/8W, ±% (R5)
2 220Ω RESISTORS, 1/4W, ±5% (R9, R11)
2 330Ω RESISTORS, 1/4W, ±5% (R10, R12)
2 510Ω RESISTORS, 1/8W, ±5% (R7, R8)

Figure 5. MULTIBUS® System Backplane Example

PHYSICAL CHARACTERISTICS (Con't)

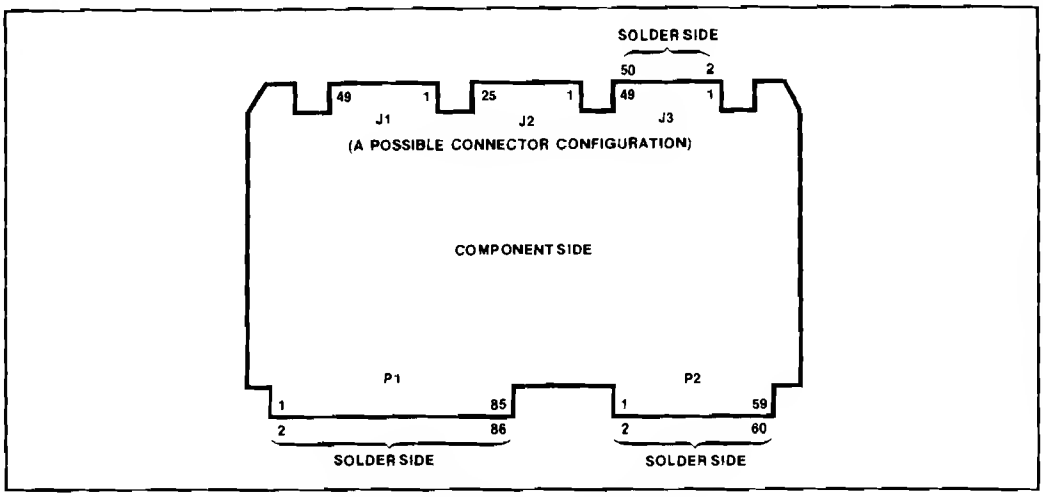


Figure 6. Connector and Pin Numbering

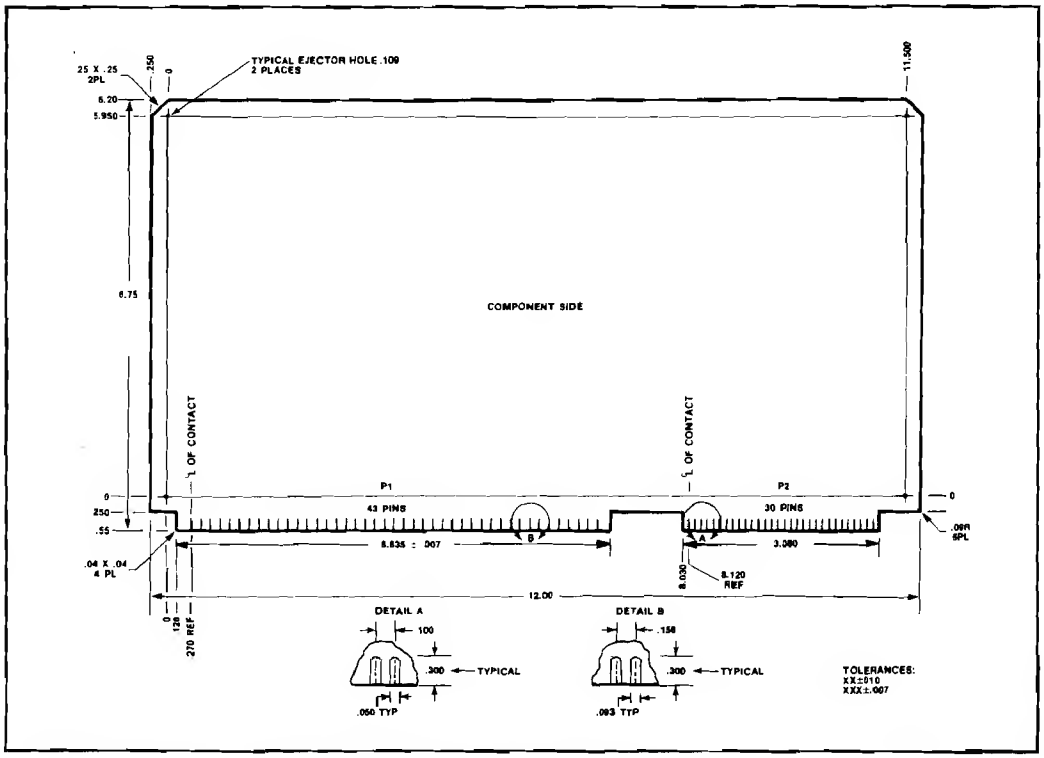


Figure 7. Standard Printed Wiring Board Outline

Backplane Connectors

Table 4. Connector Vendors

Function	# Of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
Multibus Connector (P1)	43/86	0.156	Soldered[1]	VIKING ELFAB	2KH43/9AMK12 BS1562D43PBB	102247-001
Multibus Connector (P1)	43/86	0.156	Wire wrap[2]	ELFAB ELDAC	BW1562D43PBB 3370860540201	102248-001
				ELFAB EDAC	BW1562A43PBB 337086540202	102273-001[1]
Auxiliary Connector (P2)	30/60	0.1	Soldered[1]	ELFAB EDAC	BS1020A30PBB 345060524802	102238-001
Auxiliary Connector (P2)	30/60	0.1	Wire wrap[2]	TI VIKING	H421121-30 3KH30/9JNK	N/A[3]
				EDAC ELFAB	345060540201 BW1020D30PBB	102241-001

Notes:
1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.
3. With mounting ears with .128 mounting holes.

Environmental Characteristics

Operating Temperature — 0 to 55°C; free moving air across modules and bus

Humidity — 90% maximum (no condensation)

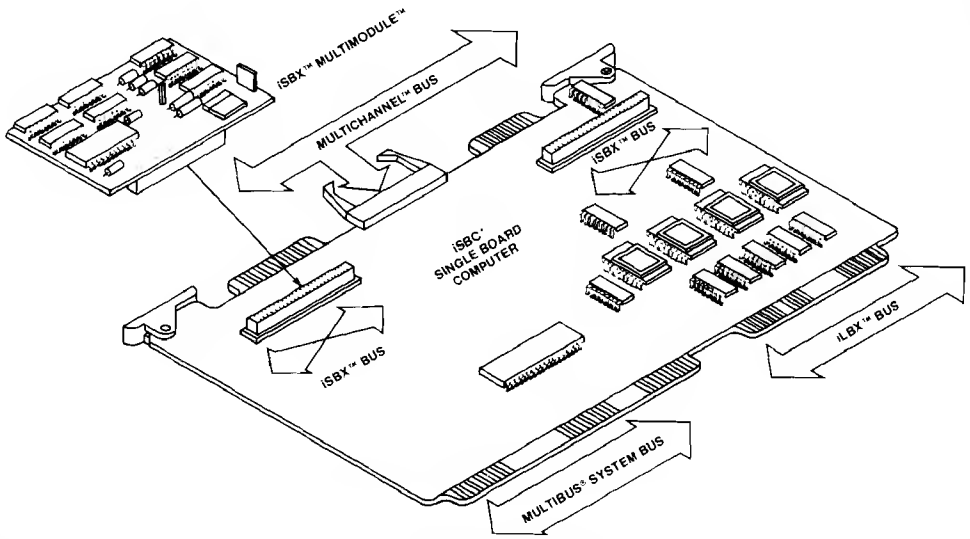
Reference Manuals

210883 — MULTIBUS Handbook

iSBX™ I/O EXPANSION BUS

- **IEEE P959 industry standard I/O expansion bus**
- **Provides on-board expansion of system resources**
- **Small iSBX™ MULTIMODULE™ boards plug directly into iSBC® boards**
- **Supports compatible 8- and 16-bit data transfer operations**
- **Part of Intel's Total System Architecture: MULTIBUS,® iLBX,™ MULTICHANNEL,™ and iSBX™**
- **Low-cost "vehicle" to incorporate the latest VLSI technology into iSBC®-based systems**
- **Provides increased functional capability and high performance**
- **Supported by a complete line of iSBC® base boards and iSBX™ MULTIMODULE™ boards, providing analog and digital I/O, high-speed math, serial and parallel I/O, video graphics, and peripheral controllers**

The iSBX™ I/O Expansion Bus is one of a family of standard bus structures resident within Intel's total system architecture. The iSBX bus is a modular, I/O expansion bus capable of increasing a single board computer's functional capability and overall performance by providing a structure to attach small iSBX MULTIMODULE™ boards to iSBC® base boards. It provides for rapid incorporation of new VLSI into iSBC MULTIBUS® systems, reducing the threat of system obsolescence. The iSBX bus offers users new economics in design by allowing both system size and system cost to be kept at minimum. As a result, the system design achieves maximum on-board performance while allowing the MULTIBUS interface to be used for other system activities. The iSBX bus enables users to add-on capability to a system as the application demands it by providing off-the-shelf standard MULTIMODULE boards in the areas of graphics controllers, advanced mathematics functions, parallel and serial I/O, disk and tape peripheral controllers, and magnetic bubble memory. A full line of MULTIBUS boards and iSBX MULTIMODULE boards are available from Intel and other third party sources in the industry.



FUNCTIONAL DESCRIPTION

Bus Elements

The iSBX™ MULTIMODULE™ system is made up of two basic elements: base boards and iSBX MULTIMODULE boards. In an iSBX system, the role of the base board is simple. It decodes I/O addresses and generates the chip selects for the iSBX MULTIMODULE boards.

The iSBX bus supports two classes of base boards, those with direct memory access (DMA) support and those without. Base boards with DMA support have DMA controllers that work in conjunction with an iSBX MULTIMODULE board (with DMA capability) to perform direct I/O to memory or memory to I/O operations. Base boards without DMA support use a subset of the iSBX bus and simply do not use the DMA feature of the iSBX MULTIMODULE board.

The iSBX MULTIMODULE boards are small, specialized, I/O mapped boards which plug into base boards. The iSBX boards connect to the iSBX bus connector and convert iSBX bus signals to a defined I/O interface.

Bus Interface/Signal Line Descriptions

The iSBX bus interface can be grouped into six functional classes: control lines, address and chip select lines, data lines, interrupt lines, option lines, and power lines. The iSBX bus provides nine control lines that define the communications protocol between base board and iSBX MULTIMODULE boards. These control lines are used to manage the general operation of the bus by specifying the type of transfer, the coordination of the transfer, and the overall state of the transfer between devices. The five address and chip select signal lines are used in conjunction with the commmand lines to establish the I/O port address being accessed, effectively selecting the proper iSBX MULTIMODULE. The data lines on the iSBX bus can number 8 or 16, and are used to transmit or receive information to or from the iSBX MULTIMODULE ports. Two interrupt lines are provided to make interrupt requests possible from the iSBX board to the base board. Two option lines are reserved on the bus for unique user requirements, while several power lines provide +5 and ±12 volts to the iSBX boards.

Bus Pin Assignments

The iSBX bus uses widely available, reliable connectors that are available in 18/36 pin for 8-bit devices and 22/44 pin for 16-bit devices. The male iSBX connector is attached to the iSBX MULTIMODULE board and the female iSBX connector is attached to the base board. Figure 2 shows the dimensions and pin numbering of the 18/36 pin iSBX connector, while Figure 3 does the same for the 22/44 pin iSBX connector. A unique scheme allows the 16-bit female connector to support 8 or 16-bit male MULTIMODULE boards. Table 1 lists the signal/pin assignments for the bus.

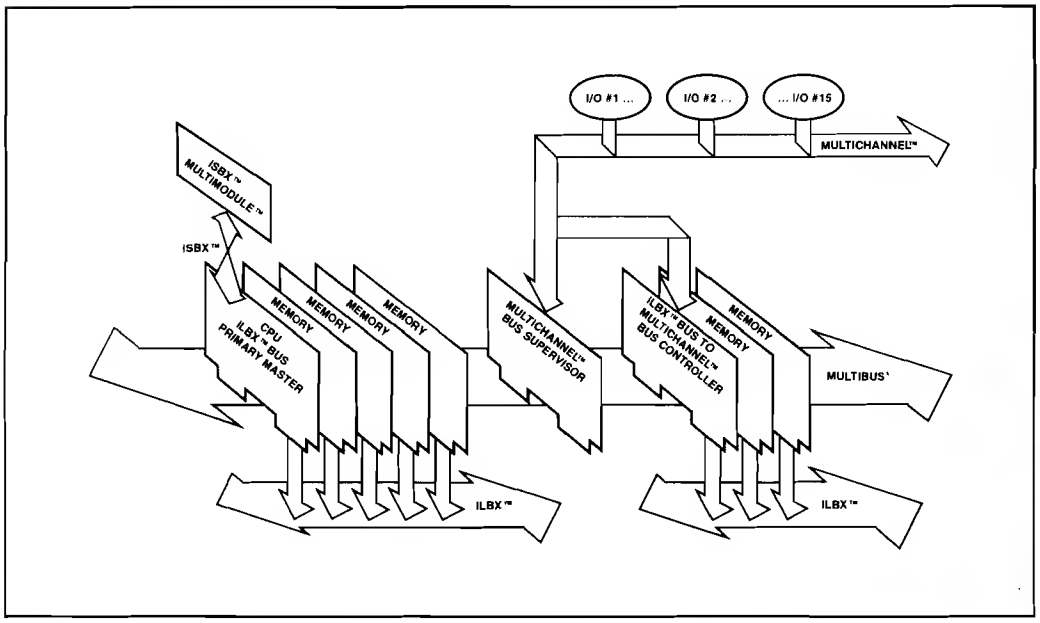


Figure 1. MULTIBUS® System Architecture

Table 1. iSBX™ Signal/Pin Assignments

Pin[1]	Menmonic	Description	Pin[1]	Mnemonic	Description
43	MD8	MDATA Bit 8	44	MD9	MDATA Bit 9
41	MDA	MDATA Bit A	42	MDB	MDATA Bit F
39	MDC	MDATA Bit C	40	MDD	MDATA Bit D
37	MDE	MDATA Bit E	38	MDF	MDATA Bit F
35	GND	Signal Gnd	36	+5V	+5 Volts
33	MD0	MDATA Bit 0	34	MDRQT	M DMA Request
31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30	OPT0	Option 0
27	MD3	MDATA Bit 3	28	OPT1	Option 1
25	MD4	MDATA Bit 4	26	TDMA	Terminate DMA
23	MD5	MDATA Bit 5	24		Reserved
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS1/	M Chip Select 1
17	GND	Signal Gnd	18	+5V	+5 Volts
15	IORD/	I/O Read Cmd	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Cmd	14	MINTR0	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		Reserved
7	MA2	M Address 2	8	MPST/	iSBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Gnd	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Notes:
1. Pins 37-44 are used only on 8/16-bit systems
2. All undefined pins are reserved for future use.

Bus Operation Protocol

COMMAND OPERATION

The iSBX bus supports two types of transfer operations between iSBX elements: I/O Read and I/O Write. An iSBX board can respond to these I/O transfers using either full speed mode or extended mode.

For a full speed I/O Read (Figure 4) the base board generates a valid I/O address and a valid chip select for the iSBX MULTIMODULE board. After set-up, the base board activates the I/O Read line causing the iSBX board to generate valid data from the addressed I/O port. The base board then reads the data and removes the read command, address, and chip select. The full speed I/O Write (Figure 5) operation is similar to the I/O Read except that the base board generates valid data on the lines and keeps the write command line active for the specified a hold time.

The extended Read operation (Figure 6) is used by iSBX MULTIMODULE boards that aren't configured to meet full speed specifications. It's operation is similar to full speed mode, but must use a wait signal to ensure proper

data transfer. The base board begins the operation by generating a valid I/O address and chip select. After set-up, the base board activates the Read line causing the iSBX board to generate a Wait signal. This causes the CPU on the base board to go into a wait state. When the iSBX board has placed valid Read data on the data lines, the MULTIMODULE board will remove the Wait signal and release the base board CPU to read the data and deactivate the command, address, and chip select. The extended Write operation (Figure 7) is similar to the extended Read except that the Wait signal is generated after the base board places valid Write data on the data lines. The iSBX board removes the Wait signal when the write pulse width requirements are satisfied, and the base board can then remove the write command after the hold time is met.

DMA OPERATION

An iSBX MULTIMODULE system can support DMA when the base board has a DMA controller and the iSBX MULTIMODULE board can support DMA mode. Burst mode DMA is fully supported, but for clarity and simplicity, only a single DMA transfer for an 8-bit base board is discussed.

A DMA cycle (Figure 8) is initiated by the iSBX board when it activates the DMA request line going to the DMA controller on the base board. When the DMA controller gains control of the base board bus, it acknowledges back to the iSBX board and activates an I/O or Memory Read. The DMA controller then activates an I/O or Memory Write respectively. The iSBX board removes the DMA request during the cycle to allow completion of the DMA cycle. Once the write operation is complete, the DMA controller is free to deactivate the write and read command lines after a data hold time.

INTERRUPT OPERATION

The iSBX MULTIMODULE board on the iSBX bus can support interrupt operations over its interrupt lines. The iSBX board initiates an interrupt by activating one of its two interrupt lines which connect to the base board. The CPU processes the interrupt and executes the interrupt service routine. The interrupt service routine signals the iSBX MULTIMODULE board to remove the interrupt, and then returns control to the main line program when the service routine is completed.

Please refer to the Intel iSBX Bus Specification for more detailed information on its operation and implementation.

SPECIFICATIONS

Word Size

Data — 8, 16-bit

Port Assignments

Table 2. iSBX™ MULTIMODULE™ Base Board Port Assignments

iSBX™ Connector Number	Chip Select	8-Bit Base Board Address	16-Bit Base Board Address (8-bit mode)	16-Bit Base Board Address (16-bit mode)
iSBX™ 1	MCS0/ MCS1/	F0-F7 F8-FF	0A0-0AF 0B0-0BF	0A0, 2, 4, 6, 8, A, C, E 0A1, 3, 5, 7, 9, B, D, F
iSBX™ 2	MCS0/ MCS1/	C0-C7 C8-CF	080-08F 090-09F	080, 2, 4, 6, 8, A, C, E 081, 3, 5, 7, 9, B, D, F
iSBX™ 3	MCS0/ MCS1/	B0-B7 B8-BF	060-06F 060-06F	060, 2, 4, 6, 8, A, C, E 061, 3, 5, 7, 9, B, D, F

Power Supply Specifications

Table 3.

Minimum (volts)	Nominal (volts)	Maximum (volts)	Maximum (current)*
+4.75	+5.0	+5.25	3.0A
+11.4	+12	+12.6	1.0A
−12.6	−12	−11.4	1.0A
—	GND	—	3.0A

* Per iSBX Multimodule board mounted on base board

DC Specifications

Table 4. iSBX™ MULTIMODULE™ Board I/O DC Specifications

Output[1]

Bus Signal Name	Type[2] Drive	I_{OL} Max −Min (mA)	@ Volts (V_{OL} Max)	I_{OH} Max −Min (μA)	@ Volts (V_{OH} Min)	C_O (Min) (pf)
MD0-MDF	TRI	1.6	0.5	−200	2.4	130
MINTR0-1	TTL	2.0	0.5	−100	2.4	40
MDRQT	TTL	1.6	0.5	− 50	2.4	40
MWAIT/	TTL	1.6	0.5	− 50	2.4	40
OPT1-2	TTL	1.6	0.5	− 50	2.4	40
MPST/	TTL	Note 3				

Input[1]

Bus Signal Name	Type[2] Receiver	I_{IL} Max (mA)	@ V_{IN} MAX (volts) Test Cond.	I_{IH} Max (μA)	@ V_{IN} MAX (volts) Test Cond.	C_I Max (pf)
MD0-MDF	TRI	−0.5	0.4	70	2.4	40
MA0-MA2	TTL	−0.5	0.4	70	2.4	40
MCS0/-MCS1/	TTL	−4.0	0.4	100	2.4	40
MRESET	TTL	−2.1	0.4	100	2.4	40
MDACK/	TTL	−1.0	0.4	100	2.4	40
IORD/ IOWRT/	TTL	−1.0	0.4	100	2.4	40
MCLK	TTL	− 2.0	0.4	100	2.4	40
OPT1-OPT2	TTL	−2.0	0.4	100	2.4	40

NOTES:
1. Per iSBX Multimodule I/O board.
2. TTL = standard totem pole output. TRI = Three-state.
3. iSBX Multimodule board must connect this signal to ground.

All Inputs. Max V_{IL} = 0.8V
Min V_{IH} = 2.0V

Connectors

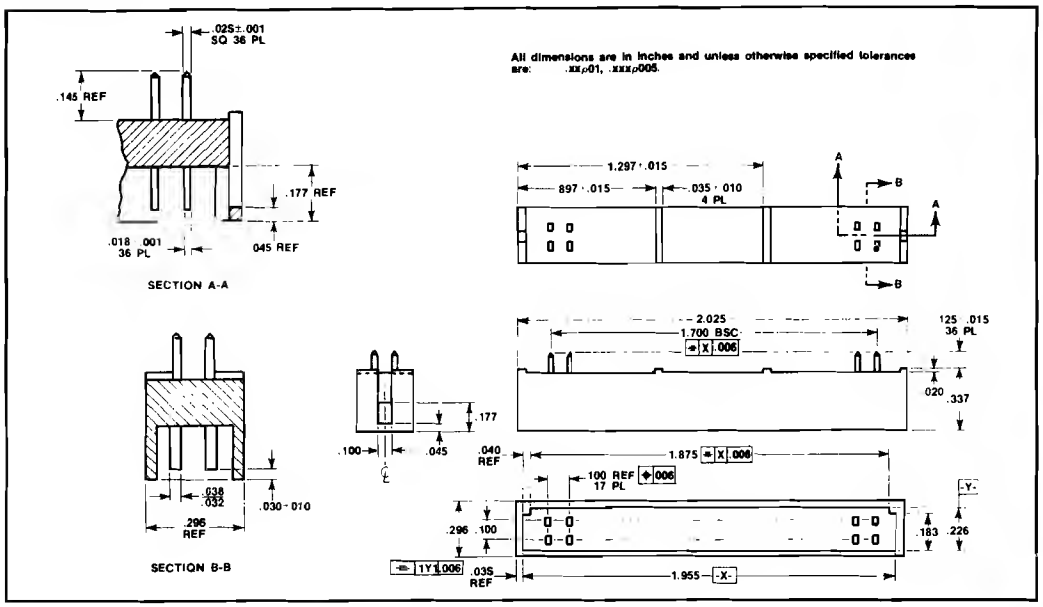


Figure 2. 18/36 Pin iSBX™ Connector

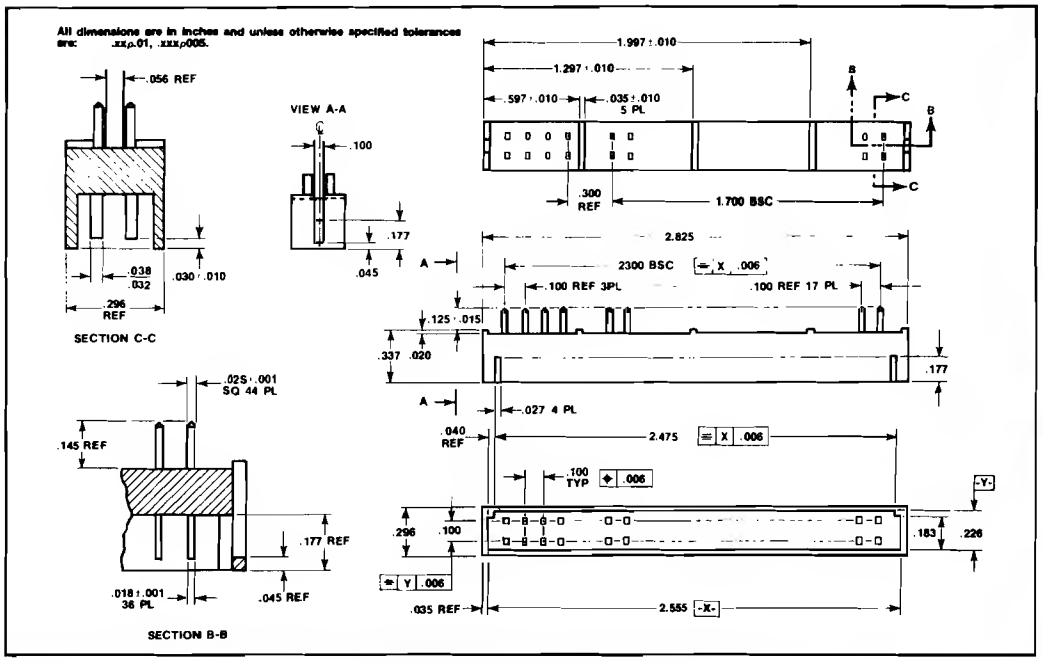


Figure 3. 22/44 Pin iSBX™ Connector

Bus Timing Diagrams

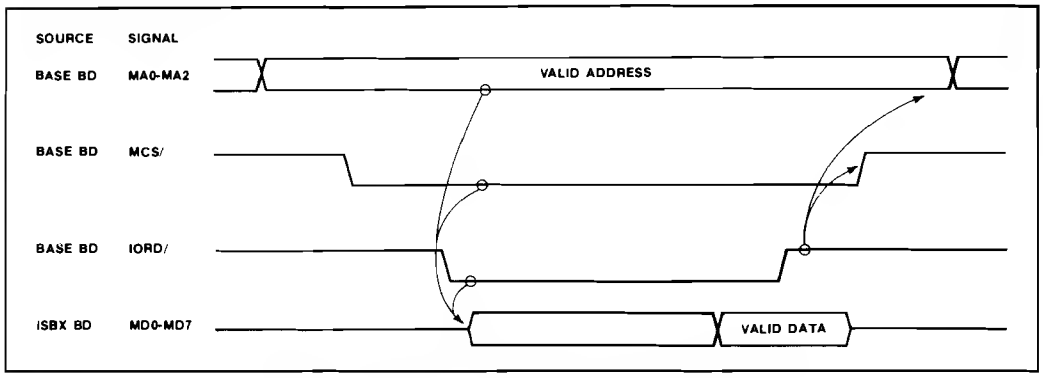


Figure 4. iSBX™ MULTIMODULE™ Read, Full Speed

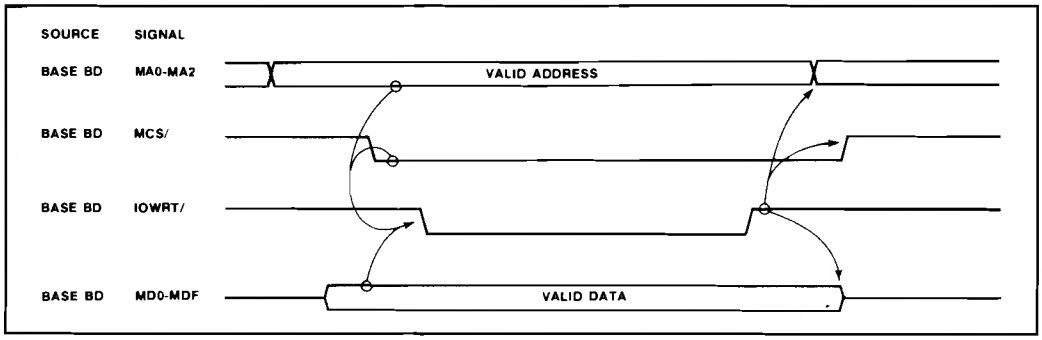


Figure 5. iSBX™ MULTIMODULE™ Board Write, Full Speed

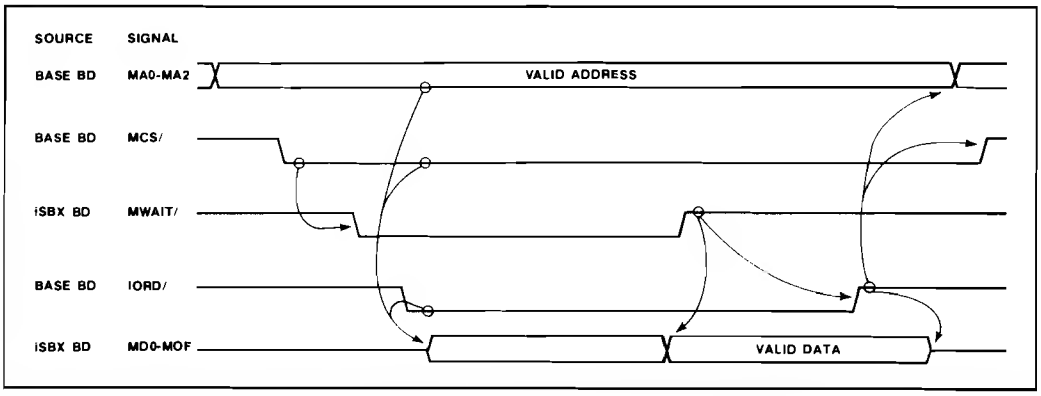


Figure 6. iSBX™ MULTIMODULE™ Board Extended Read

Bus Timing Diagram (Con't)

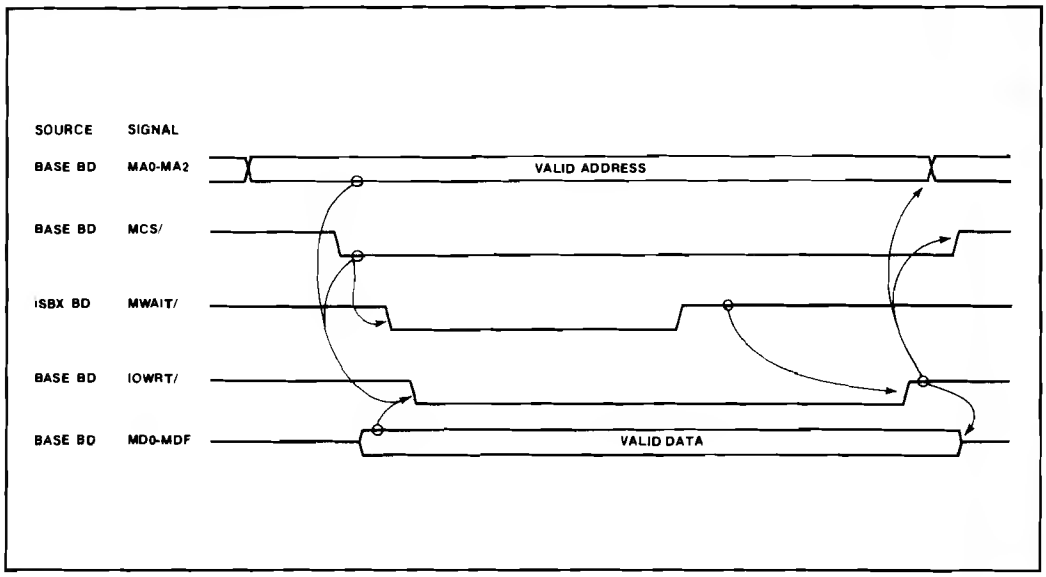


Figure 7. iSBC™ MULTIMODULE™ Board Extended Write

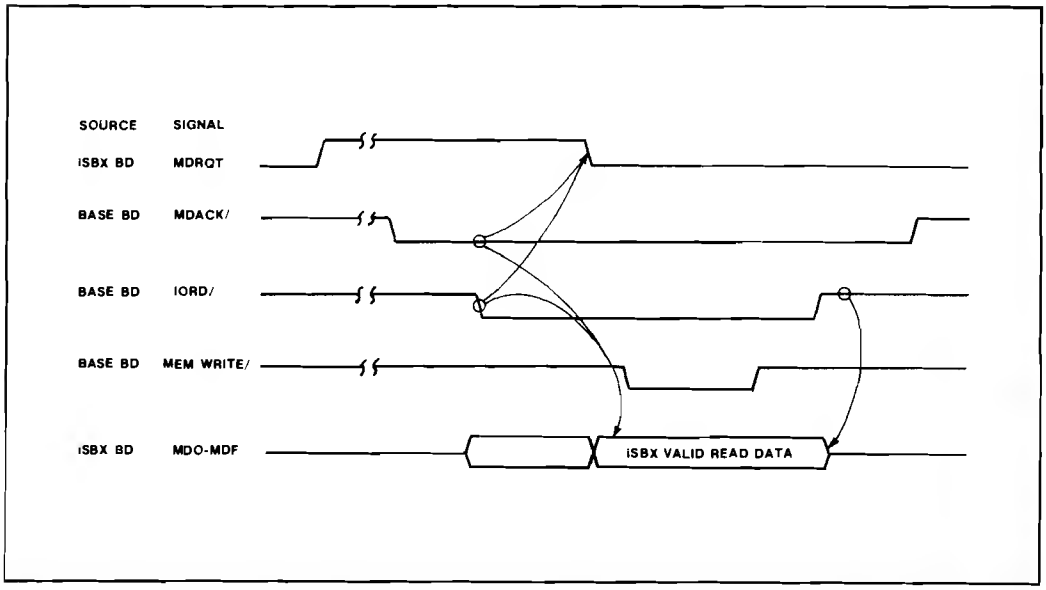


Figure 8. iSBX™ MULTIMODULE™ Board DMA Cycle (iSBX™ MULTIMODULE™ to Base Board Memory)

Board Outlines

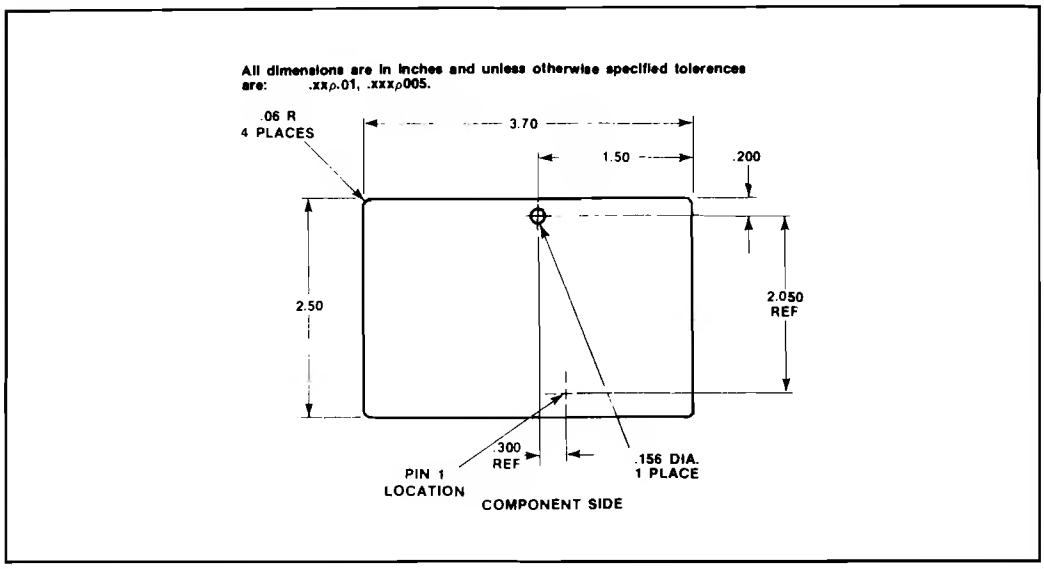


Figure 9. iSBX™ Board Outline

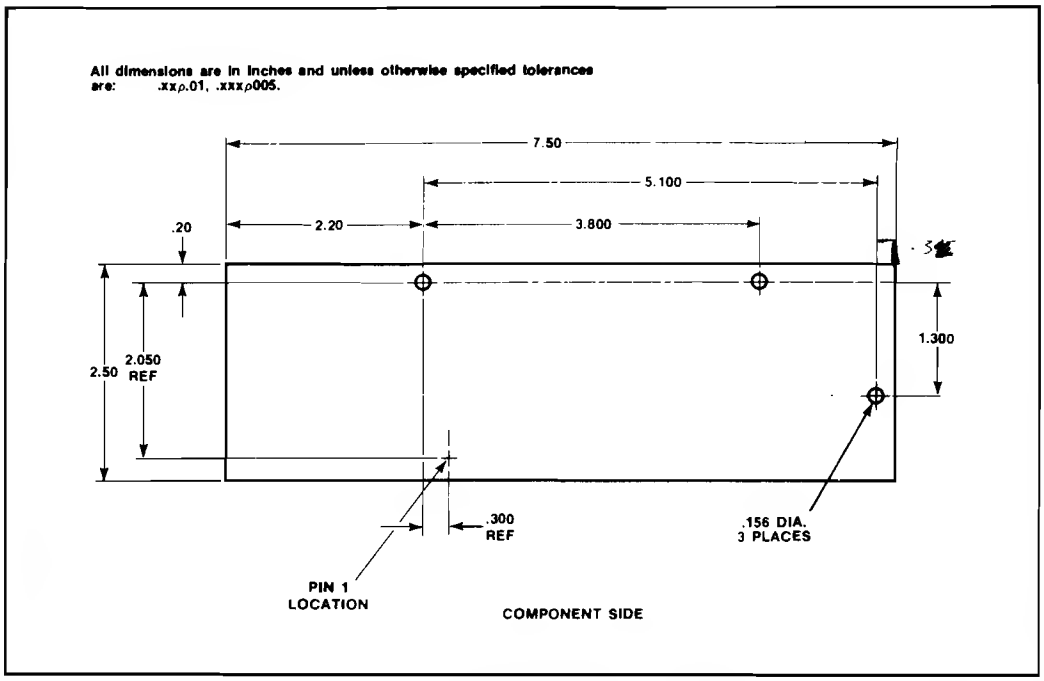


Figure 10. Double Wide iSBX™ Board Outline

Environmental Characteristics

Operating Temperature — 0 to 55°C

Humidity — 90% maximum relative; non-condensing

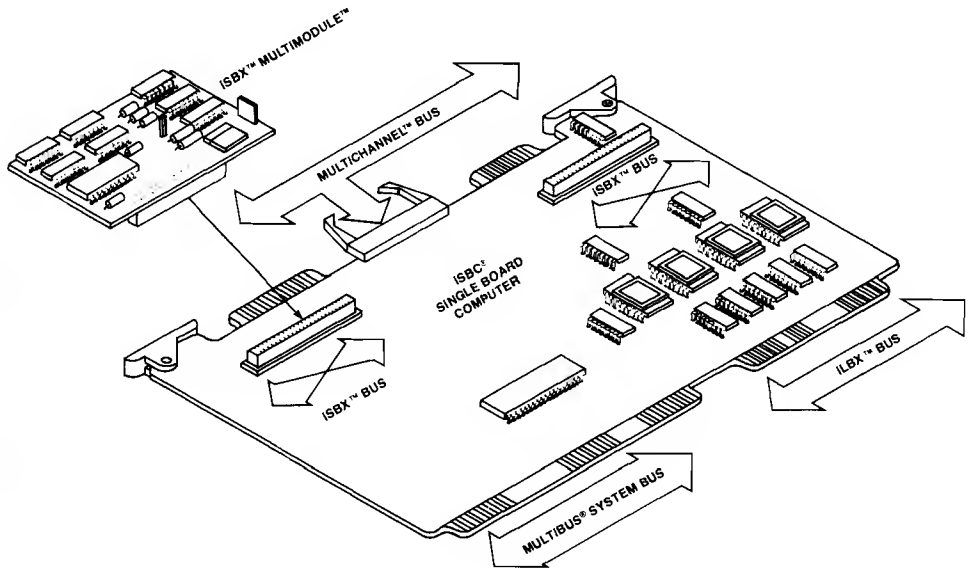
Reference Manuals

210883 — MULTIBUS Handbook

iLBX™ EXECUTION BUS

- **High bus bandwidth**
  - **— 9.5 Mbytes/sec. for 8-bit transfers**
  - **— 19 Mbytes/sec. for 16-bit transfers**
- **16 Mbyte addressing range**
- **8 and 16-bit data transfers**
- **Supports up to 5 iLBX™ compatible devices per bus**
- **Primary and secondary master bus exchange capabilities**
- **Standard 60-pin MULTIBUS® P2 connector**

The iLBX™ Execution Bus is one of a family of standard bus structures resident within Intel's total system architecture. The Local Bus Extension (iLBX) Bus is a dedicated execution bus capable of significantly increasing system performance by extending the processor board's on-board local bus to off-board resources. This extension provides for arbitration-free, direct access to high-performance memory. Acting as a "virtual" iSBC®, up to 16 megabytes of processor addressable memory can be accessed over the iLBX bus and appear as though it were resident on the processor board. The iLBX Bus preserves advantages in performance and architecture of on-board memory, while allowing memory configurations larger than possible on a single board computer. High throughput and independence from MULTIBUS® activities make the iLBX bus an ideal solution for "working store" type program memory and data processing applications requiring large amounts of high performance memory. Such applications include graphics systems, robotics, process control, office systems, and CAD/CAM.



FUNCTIONAL DESCRIPTION

Architectural Overview

The iLBX bus is an architectural solution for supporting large amounts of high performance memory. It is the first structure that allows the CPU board selection to be decoupled from the on-board memory requirement, and still maximizes the processor's performance potential. It eliminates the processor's need to access its off-board memory resources solely over the MULTIBUS system bus. Architectural consistency with the single board computer approach including iLBX memory can be maintained by dual port access of memory resources between the iLBX bus and the MULTIBUS system bus. This allows for global access by other processors and I/O devices while still providing high speed local CPU operations. This sub-system created by the iLBX bus of a single board computer and a maximum of 4 memory cards can be perceived architecturally as a "virtual single board computer". The implementation of iLBX bus "virtual modules" makes it possible to create functional modules with a new level of flexibility and performance in implementing a wide range of memory capabilities. With future needs in mind, the iLBX bus has the capability of accessing a full 16 megabytes of memory.

Structural Features

The iLBX bus uses a non-multiplexed 16-bit configuration capable of 8 and 16-bit transfers. Used in conjunction with the MULTIBUS interface, the iLBX bus resides on the MULTIBUS form factor P2 connector and supercedes the MULTIBUS interface definitions for the P2 signals. The iLBX bus uses the standard 60-pin MULTIBUS P2 connector and occupies 56 of the P2 connector pins with I6 data lines, 24 address lines plus control, command access, and parity signals. The four MULTIBUS address extension lines on the MULTIBUS/iLBX P2 connector retain the standard MULTIBUS interface definition.

Bus Elements

The iLBX bus supports three distinct device categories: 1) Primary Master, 2) Secondary Master, 3) Slave. These three device types may be combined to create several iLBX local busses ranging (in size) from a minimum of two to a maximum of five devices per iLBX bus. There is only one Primary Master in any given implementation of iLBX bus, and its presence is required along with the attachment of at least one Slave device. To provide alternate access over an iLBX bus, one optional Sec-

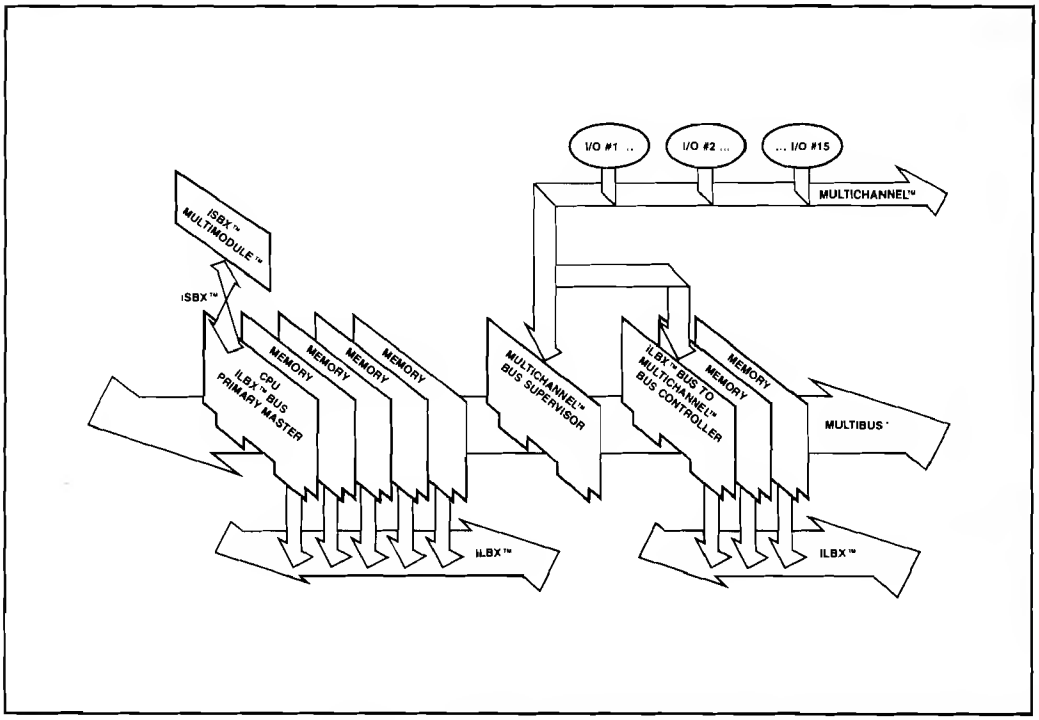


Figure 1. MULTIBUS® System Architecture

AFN-00074A

ondary Master may be incorporated to create a "two-master" local bus subsystem. By limiting the iLBX bus to two masters (a Primary and a Secondary), bus arbitration is reduced to a simple request and acknowledge process, with privileged use of the bus maintained by the Primary Master, and limited access granted to the Secondary Master when needed.

The Primary Master executes the role of iLBX bus "supervisor" by controlling the general operation of the bus and managing Secondary Master accesses to the Slave memory resources.

The Secondary Master Device is an option providing alternate access to the Slave resources on the iLBX bus. Secondary master devices are typically DMA driven. This feature is provided for implementation flexibility when occasional DMA transfers in and out of iLBX memory resources can optimize the overall system performance. The Secondary Master essentially duplicates the Primary Master's data transfer capability, but must rely on the Primary Master to grant access. Once access is granted, the Secondary Master controls the bus, and drives all signal lines until the operation is complete and control is passed back to the Primary Master.

The Slave devices contain the memory resources used by the Primary Master and the optional Secondary Master. Each iLBX implementation can contain a maximum of four Slave devices. Using 64K RAM technology on four slave devices with ECC can provide for over 2 megabytes of "on-board" high performance memory. With 256K RAM chips, each iLBX bus could contain slave devices with memory totalling 8 megabytes. As memory technology increases, the iLBX bus is designed to incorporate it in rapid fashion because it is capable of directly accessing a full 16 megabytes of memory on its high-performance Slave devices.

Bus Interface/Signal Line Descriptions

The iLBX bus interface is divided into four functional classes of signal lines: address and data lines, control lines, command lines, and bus access lines. The 40 address and data lines defined by the iLBX Bus Specification consist of 16 data lines and 24 address lines.

There are 16 bi-directional data lines exclusively used to handle 8-bit and 16-bit data transfers between the active bus master and the selected slave device. The iLBX bus uses these data lines for all data transfers, and are driven by tri-state drivers.

The 24 address lines on the iLBX bus provide the ability to directly address 16 megabytes of memory. These single-direction address lines are exclusively driven by the active bus master. The iLBX bus master uses them to select a specific slave device. Three control lines specify the type of data transfer between master and slave devices, while the three command lines initiate, control, and terminate the transfer. There are also three bus access lines used to transfer bus control between master devices.

Bus Pin Assignments

The iLBX bus uses the standard 60-pin MULTIBUS P2 connector. The physical location of each pin assignment and its corresponding function is listed in Table 1.The four MULTIBUS address extension lines (pins 55-58 on the P2 connector) retain the standard MULTIBUS interface functions.

Bus Operation Protocol

The operation protocol for the iLBX bus is a straightforward set of procedures consisting of three basic operations: bus control access, write data to memory, read data from memory. These operations use asynchronous protocol with positive acknowledgment.

Bus Access

The iLBX bus is shared by at most two masters; one Primary Master and one optional Secondary Master, each providing an alternate access path to iLBX bus memory resources. The mechanism for obtaining bus access is a simple request and acknowledge process communicated between masters. Each master is a bus controller of similar capabilities, responsible for data transfer operations between devices, but the Primary Master has the added responsibility of controlling iLBX bus accesses.

The Primary Master has default control of the iLBX bus. If the Secondary Master needs access to the bus, it must initiate a request and wait for acknowledgment from the Primary Master. The choice of when to surrender control of the bus rests with the Primary Master, but if no data transfer is in progress, the Primary Master normally relinquishes control immediately to the Secondary Master.

Data Transfer Operation

The iLBX bus supports two types of data transfer operations: write data to memory and read data from memory. These data transfer operations facilitate the passing of information between the active bus master and the selected slave device. The operation of these two transfer types is very similar; the only differences being the direction of the data transfer and the device driving the data lines.

For either type of data transfer, the active bus master first initiates the transfer operation by placing the memory address on the address lines (AB23-AB0) and a con-

trol configuration on the control lines to select the slave device. Once the slave device is selected, the type of data transfer becomes the key factor. With the write operation, the active master maintains control of the data lines and provides valid data within the specified time. Upon accepting a data element, the slave sends a receipt acknowledgment signal to the master which completes the data transfer operation.

With the read operation, the slave device drives the data lines and places valid data on the data lines before sampling by the active master. The slave acknowledges the master to signal the end of the data transfer, and the master completes the operation.

The iLBX Bus Specification includes provisions for both optimized and non-optimized data transfers. Optimized

Table 1. iLBX™ Bus Pin Assignments, P2 Edge Connector

Component Side			Solder Side		
16-Bit Pin	**Mnemonic**	**Signal Name**	**16-Bit Pin**	**Mnemonic**	**Signal Name**
1	DB0	DATA LINE 0	2	DB1	DATA LINE 1
3	DB2	DATA LINE 2	4	DB3	DATA LINE 3
5	DB4	DATA LINE 4	6	DB5	DATA LINE 5
7	DB6	DATA LINE 6	8	DB7	DATA LINE 7
9	GND	GROUND	10	DB8	DATA LINE 8
11	DB9	DATA LINE 9	12	DB10	DATA LINE 10
13	DB11	DATA LINE 11	14	DB12	DATA LINE 12
15	DB13	DATA LINE 13	16	DB14	DATA LINE 14
17	DB15	DATA LINE 15	18	GND	GROUND
19	AB0	ADDRESS LINE 0	20	AB1	ADDRESS LINE 1
21	AB2	ADDRESS LINE 2	22	AB3	ADDRESS LINE 3
23	AB4	ADDRESS LINE 4	24	AB5	ADDRESS LINE 5
25	AB6	ADDRESS LINE 6	26	AB7	ADDRESS LINE 7
27	GND	GROUND	28	AB8	ADDRESS LINE 8
29	AB9	ADDRESS LINE 9	30	AB10	ADDRESS LINE 10
31	AB11	ADDRESS LINE 11	32	AB12	ADDRESS LINE 12
33	AB13	ADDRESS LINE 13	34	AB14	ADDRESS LINE 14
35	AB15	ADDRESS LINE 15	36	GND	GROUND
37	AB16	ADDRESS LINE 16	38	AB17	ADDRESS LINE 17
39	AB18	ADDRESS LINE 18	40	AB19	ADDRESS LINE 19
41	AB20	ADDRESS LINE 20	42	AB21	ADDRESS LINE 21
43	AB22	ADDRESS LINE 22	44	AB23	ADDRESS LINE 23
45	GND	GROUND	46	ACK*	SLAVE ACKNOWLEDGE
47	BHEN	BYTE HIGH ENABLE	48	R/W	READ NOT WRITE
49	ASTB*	ADDRESS STROBE	50	DSTB*	DATA STROBE
51	SMRQ*	SECONDARY MASTER REQUEST	52	SMACK*	SECONDARY MASTER ACKNOWLEDGE
53	LOCK*	ACCESS LOCK	54	GND	GROUND
55	ADR22*	MULTIBUS® ADDRESS EXTENSION LINE 22	56	ADR23*	MULTIBUS® ADDRESS EXTENSION LINE 23
57	ADR20*	MULTIBUS® ADDRESS EXTENSION LINE 20	58	ADR21*	MULTIBUS® ADDRESS EXTENSION LINE 21
59	RES	RESERVED	60	TPAR*	TRANSFER PARITY

operation uses pipelining and signal overlapping techniques to manage the data transfer timing relationships between the active bus master and the selected slave. The use of signal overlapping requires that every device attached to the iLBX bus provide a means for varying the timing of the slave request and acknowledge signals. The non-optimized operation uses fixed signal sequences, instead of signal overlapping, to assure a valid data transfer, and a device does not need a variable request or acknowledge to read data-valid timing on the iLBX bus. Please refer to the iLBX Bus Specification for detailed descriptions of these transfer operations.

Mechanical Implementation

Because the iLBX bus uses the P2 connector of the MULTIBUS form factor, the iLBX bus "shares" a MULTIBUS chassis with the MULTIBUS backplane system bus in the system design. The iLBX mechanical specifications are synonymous with the MULTIBUS specifications for board-to-board spacing, board thickness, component lead length, and component height above the board. The iLBX bus interconnection can use either flexible ribbon cable or a rigid backplane. The iLBX bus interconnect maximum length is limited to 10 cm (approximately 4 inches); that is sufficient to span 5 card slots across two connected chassis. Figure 2 shows an iLBX bus cable assembly.

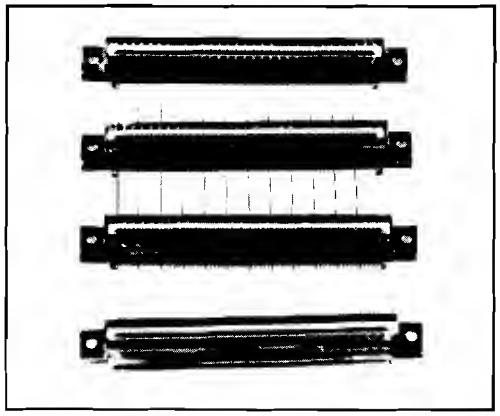


Figure 2. Typical iLBX™ Bus Interface Cable Assembly

SPECIFICATIONS

Word Size

Data — 8 and 16-bit

Memory Addressing

24-bits – 16 megabyte – direct access

Bus Bandwidth

9.5 megabytes/sec — 8-bit

19 megabytes/sec — 16-bit

Electrical Characteristics

DC SPECIFICATIONS

Table 2. DC Specifications

Signal Name	Driver Type	Termination (to +5 Vdc) At Master	Min. Driver Requirements			Max. Receiver Requirements		
			High	Low	Load Cap.	High	Low	Load Cap.
DB15-0	TRI-STATE	10K Ohms	0.4 ma	9 ma	75 pf	0.15 ma	2 ma	18 pf
TPAR*	TRI-STATE	10K Ohms	0.4 ma	9 ma	75 pf	0.15 ma	2 ma	18 pf
AB23-0	TRI-STATE	None	0.4 ma	20 ma	120 pf	0.10 ma	5 ma	30 pf
R/W	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
BHEN	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
LOCK*	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
SMRQ*	TTL	10K Ohms	0.05 ma	8 ma	20 pf	0.05 ma	2 ma	18 pf
SMACK*	TTL	None	0.05 ma	2 ma	20 pf	0.05 ma	2 ma	18 pf
†ASTB*	TRI-STATE	10K Ohms	0.2 ma	9 ma	75 pf	0.05 ma	2 ma	18 pf
†DSTB*	TRI-STATE	10K Ohms	0.2 ma	9 ma	75 pf	0.05 ma	2 ma	18 pf
ACK*	OPEN COLL.	330 Ohms	N.A.	20 ma	45 pf	0.05 ma	2 ma	18 pf

† At slave, series RC termination to GND (100 ohm, 10 pf)

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BUS TIMING

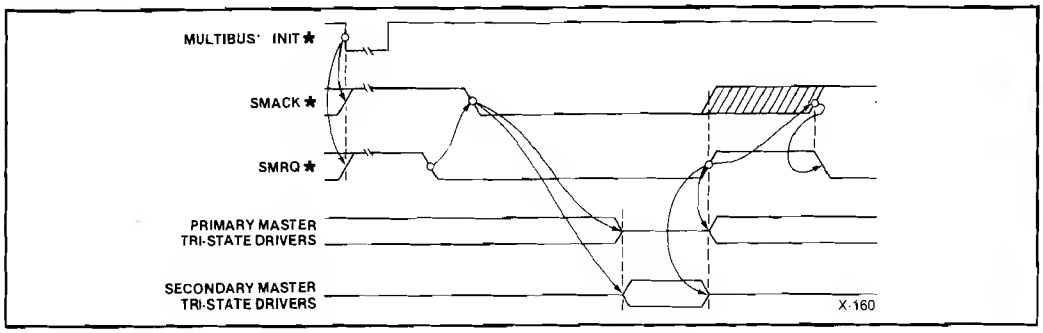

Figure 3. iLBX™ Bus Granting Timing Chart

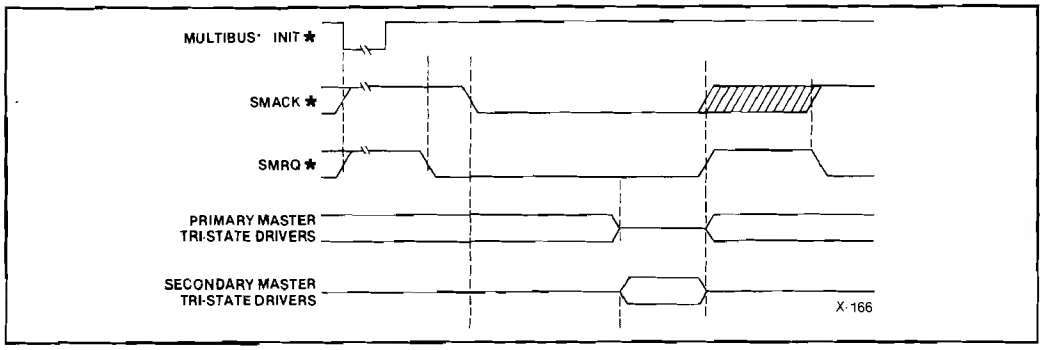

Figure 4. iLBX™ Bus Control Transfer Timing Chart

16-Bit Transfer Timing —

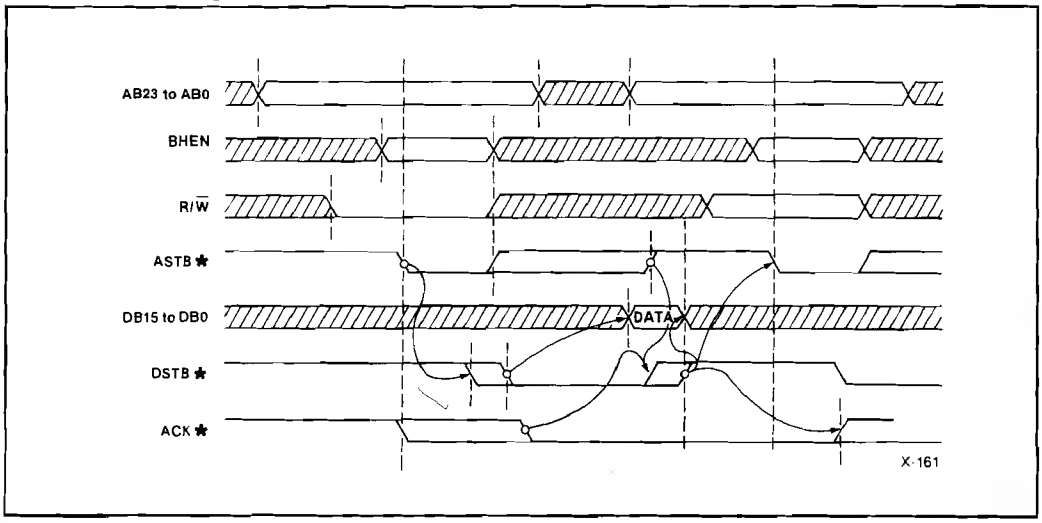

Figure 5. Write Data-To-Memory

BUS TIMING

16-Bit Transfer Timing (Con't.) —

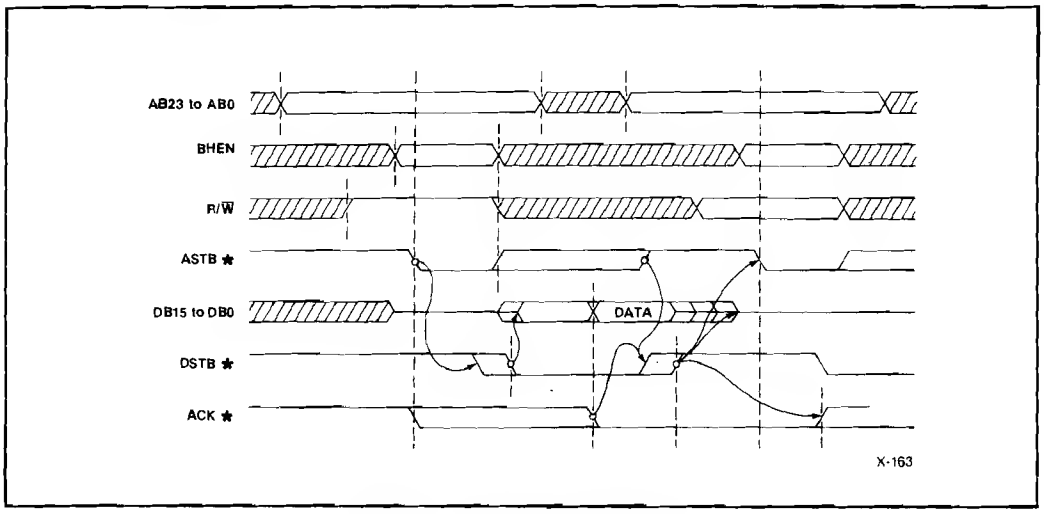

Figure 6. Read Data-From-Memory

Physical Characteristics

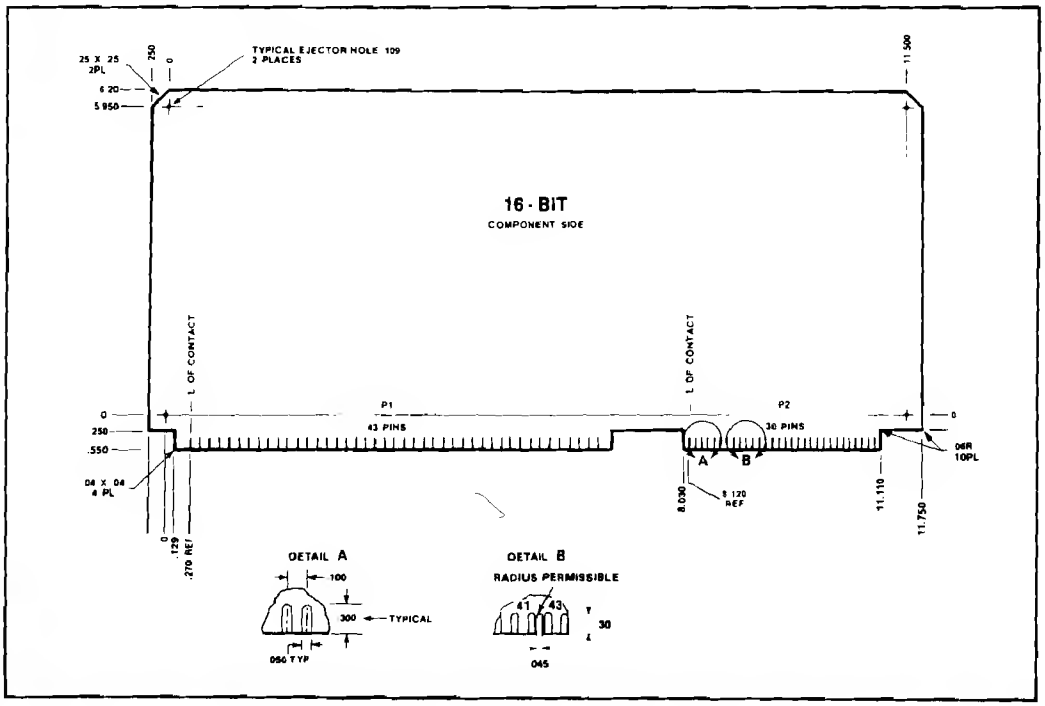

Figure 7. ILBX™ Bus Standard Printed Circuit Board Outline

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Cables and Connectors

Table 3. Cable and Receptacle Vendors

iLBX™ Bus Compatible Cable		
Vendor	**Vendor Part No.**	**Conductors**
T&B Ansley	171-60	60
T&B Ansley	173-60	60
3M	3365/60	60
3M	3306/60	60
Berg	76164-060	60
Belden	9L28060	60
Spectrastrip	455-240-60	60
iLBX™ Bus Compatible Receptacles		
Vendor	**Vendor Part No.**	**Pins**
Kelam	RF30-2803-5	60
T&B Ansley	A3020 (609-6025 modified)	60

Environmental Characteristics

OPERATING

Temperature — 0 to 55°C

Relative Humidity — 0 to 85 percent; non-condensing

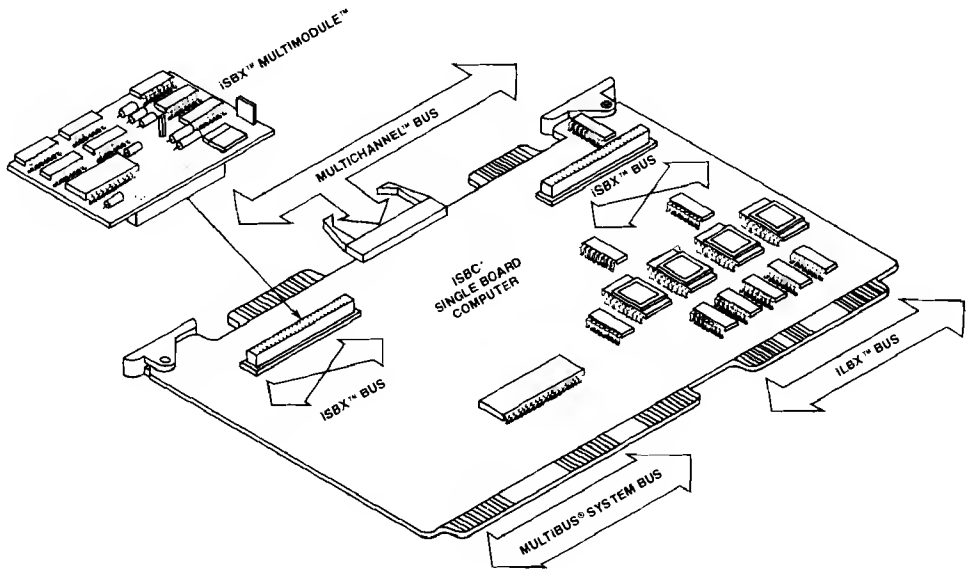
Reference Manuals

210883 — MULTIBUS Handbook

MULTICHANNEL™ I/O BUS

- **High speed 8- or 16-bit block transfers between memory and/or I/O**
- **Transfer rates up to 8 megabytes/sec.**
- **Full speed operation at distances of up to 15 meters.**
- **Supports Supervisor, Controller, or basic Talker/Listener capabilities**
- **Off-loads burst mode I/O activities from host CPU and MULTIBUS® system bus**
- **Up to 16 devices may be interfaced to the bus.**
- **16 megabytes of memory and 16 megabytes of I/O are addressable on each device**

The MULTICHANNEL™ I/O Bus is one of a family of standard bus structures resident within Intel's total system architecture. The MULTICHANNEL bus is a general purpose, high-speed I/O bus capable of significantly increasing system performance by providing a separate data path for DMA I/O activities. By isolating I/O transfers from the system bus, the MULTICHANNEL bus off-loads I/O activity from the host CPU, reduces the probability of bus saturation on the system bus, and reduces contention between I/O and data processing activities on the system bus. The MULTICHANNEL bus can support up to 16 devices at distances up to 15 meters with a maximum burst throughput of 8 megabytes per second. These 16 devices are classified in a manner similar to the IEEE 488 bus concept: Supervisors, Controllers, or Talker and Listeners. As a non-proprietary, standardized I/O bus, the MULTICHANNEL bus is a cost-effective DMA interface ideal for applications such as computer graphics, specialized peripheral control, automatic test equipment, video camera image processing, data acquisition, and high-speed MULTIBUS® system-to-system communication.



FUNCTIONAL DESCRIPTION

Architectural Overview

The MULTICHANNEL bus is the standard high speed I/O interface to MULTIBUS-based systems. Its general purpose design and high performance (8 MB/sec) augment the overall system design by improving I/O interface flexibility and system throughput. The flexibility is realized by using an easy-to-use public standard interface that can support up to sixteen 8-bit or 16-bit devices at up to 15 meters. This structure allows the MULTICHANNEL bus to provide easy I/O system expansion, effective box-to-box communication, and a growth path capable of supporting new generations of high-performance I/O devices. The MULTICHANNEL bus increases system throughput by providing a high-performance data path for efficient movement of large amounts of data.

Structural Features

MULTICHANNEL™ BUS CONFIGURATION

The MULTICHANNEL bus is a multiplexed, asynchronous block transfer, 16-bit I/O bus designed to handle 8-bit and 16-bit transfers between peripherals and single board computers. Its structure (pictured in Figure 2) consists of 16 address/data lines, 6 control lines, 2 interrupt lines, plus parity and reset. These signal lines are implemented as either a 60 conductor flat ribbon cable or a twisted-pair cable spanning a distance of up to 15 meters. A 30/60-pin 3M® connector is recommended for device connection to the MULTICHANNEL bus. The male connectors are installed on each MULTICHANNEL device and the female connectors are mounted on the cable. To insure system integrity, the MULTICHANNEL cable is terminated at both ends.

BUS ELEMENTS

Three device types — the Basic device, the bus Controller device, and the bus Supervisor device — each provide a different level of capability. The Basic Talker/Listener device has lowest capability, responding only to data transfer requests issued by a Supervisor or Controller. The bus Controller device has higher capability than a Basic Talker/Listener on the bus. It can respond to data transfer requests, control data transfers, and can program other MULTICHANNEL devices under direction from a bus Supervisor. Operating at the highest capability is the bus Supervisor device. It provides major control and management of the MULTICHANNEL bus. The bus Supervisor resolves and grants MULTICHANNEL bus priority, monitors bus status, handles interrupts, and controls the reset line, in addition to performing all bus Controller functions.

3M is a registered trademark of 3M Corporation.

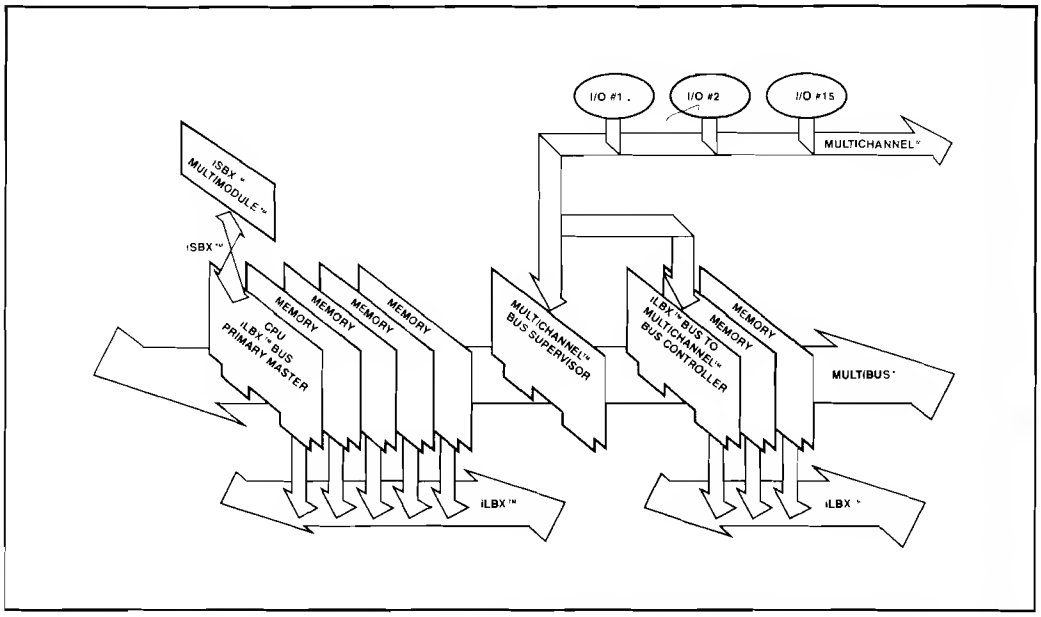


Figure 1. MULTIBUS® System Architecture

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MULTICHANNEL bus devices are functionally flexible, creating overlaps between types of bus functions and types of bus devices performing those functions. These devices perform functions in various states of operation: master, slave, talker, listener. When a device is controlling the command/action lines, it is in the master state, and both the bus Supervisor and the bus Controller can operate in this state, although not simultaneously. The slave state indicates a device that can monitor the command/action lines. Only Controllers and Basic Talker/Listeners operate as slaves. All three device types can operate in the talker state or the listener state, but not all at the same time. A Talker is any device selected by the bus master which is writing data to the bus. A Listener is any selected device which is reading data from the bus.

BUS INTERFACE/SIGNAL LINE DESCRIPTIONS

The MULTICHANNEL bus signal lines are grouped into five classes based on the functions they perform: address/data, control, interrupt, parity, and reset. The 16 address/data lines are multiplexed by a control line to act either as 16 unidirectional address lines or 16 bidirectional data lines. When used as address lines, they transmit the device address to all devices attached to the MULTICHANNEL bus. When used as bidirectional data lines, they transmit and receive data to or from MULTICHANNEL devices. The six control lines determine the overall operation of the bus from specifying the type of data transfer to providing the handshake for data transfers between MULTICHANNEL devices. Two interrupt lines are supplied to initiate and terminate data transfers, and to indicate device failures, memory failures, or parity errors. A parity line and a reset line provide support for a parity option and system reset capability whenever required.

BUS PIN ASSIGNMENTS

For proper MULTICHANNEL implementation, a 60 conductor (twisted pair or flat) cable using a 30/60 pin 3M connector, is used for device connection to the bus. Figure 3 is an outline drawing of the iSBC® MULTICHANNEL connector which also shows the pin numbering. The MULTICHANNEL bus connector signal pin assignments are listed in Table 1. Cable termination is implemented at both cable ends to insure proper system integrity over a 15-meter cable. Figure 4 is a schematic of the cable termination circuits. A cable termination module could be created that would then be connected to the cable end via a 30/60 pin connector.

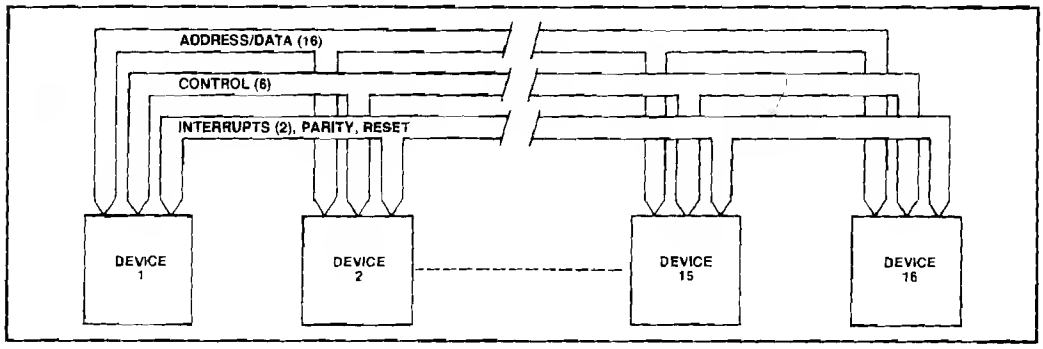

Figure 2. Block Diagram of MULTICHANNEL™ Bus Structure

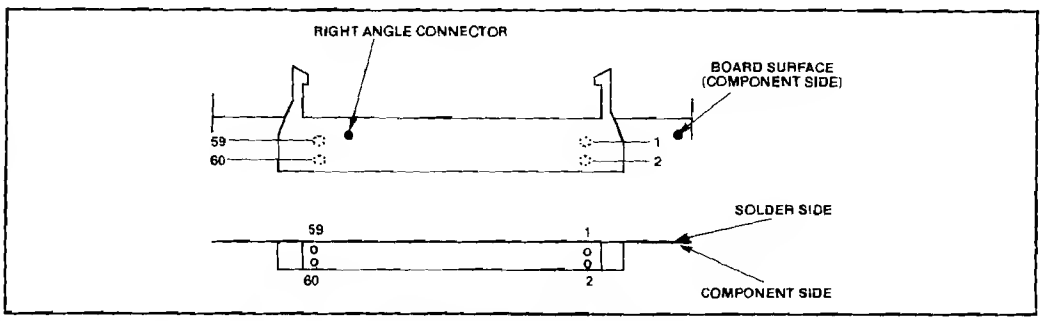

Figure 3. Connector Example

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Table 1. MULTICHANNEL™ Bus Pin Assignments

Lower Row			Upper Row		
Pin	**Mnemonic**	**Signal Name**	**Pin**	**Mnemonic**	**Signal Name**
1	GND	GROUND	2	AD0/	ADDRESS DATA LINE 0
3	GND	GROUND	4	AD1/	ADDRESS DATA LINE 1
5	GND	GROUND	6	AD2/	ADDRESS DATA LINE 2
7	GND	GROUND	8	AD3/	ADDRESS DATA LINE 3
9	GND	GROUND	10	AD4/	ADDRESS DATA LINE 4
11	GND	GROUND	12	AD5/	ADDRESS DATA LINE 5
13	GND	GROUND	14	AD6/	ADDRESS DATA LINE 6
15	GND	GROUND	16	AD7/	ADDRESS DATA LINE 7
17	GND	GROUND	18	AD8/	ADDRESS DATA LINE 8
19	GND	GROUND	20	AD9/	ADDRESS DATA LINE 9
21	GND	GROUND	22	ADA/	ADDRESS DATA LINE 10
23	GND	GROUND	24	ADB/	ADDRESS DATA LINE 11
25	GND	GROUND	26	ADC/	ADDRESS DATA LINE 12
27	GND	GROUND	28	ADD/	ADDRESS DATA LINE 13
29	GND	GROUND	30	ADE/	ADDRESS DATA LINE 14
31	GND	GROUND	32	ADF/	ADDRESS DATA LINE 15
33	GND	GROUND	34	RESET/	RESET
35	GND	GROUND	36	AACC	ADDRESS MODE ACCEPT
37	GND	GROUND	38	SRQ/	SERVICE REQUEST
39	GND	GROUND	40	STO/	SUPERVISOR TAKE OVER
41	GND	GROUND	42	DACC/	DATA MODE ACCEPT
43	GND	GROUND	44	SA/	SUPERVISOR ACTIVE
45	PB*/	PARITY BIT (INV.)	46	PB/	PARITY BIT
47	R/W/	READ NOT WRITE (INV.)	48	R/W	READ NOT WRITE
49	A/D/	ADDRESS NOT DATA (INV.)	50	A/D	ADDRESS NOT DATA
51	DRDY*/	DATA READY (INV.)	52	DRDY/	DATA READY
53	RES	RESERVED	54	RES	RESERVED
55	RES	RESERVED	56	RES	RESERVED
57	RES	RESERVED	58	RES	RESERVED
59	RES	RESERVED	60	RES	RESERVED

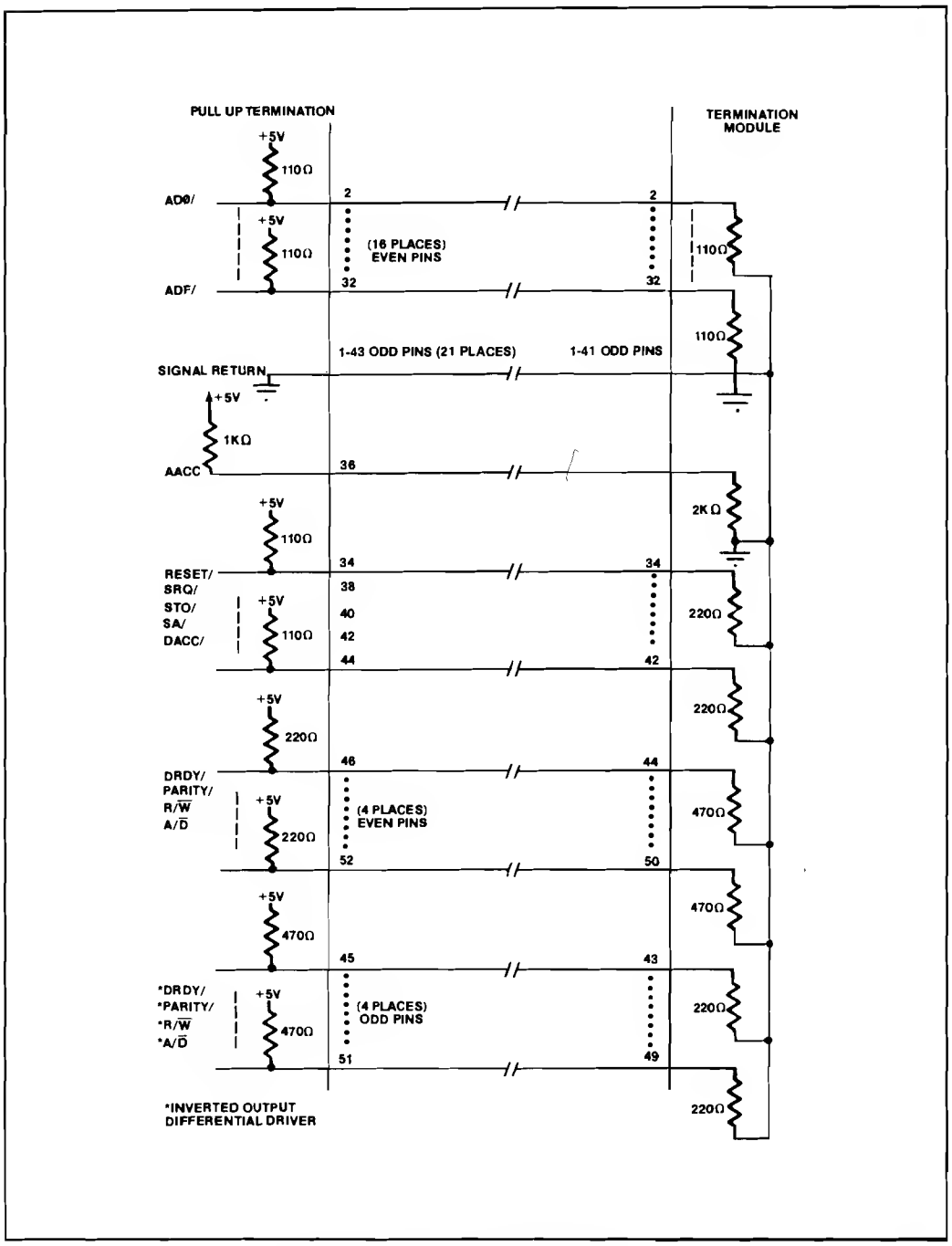

Figure 4. Bus Termination Schematic

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Bus Operation Protocol

DATA TRANSFER OPERATION

There are three modes of communication in the operation protocol: address mode, data mode, and control transfer mode. Using these transfer modes, each MULTICHANNEL device provides handshaking capability for totally asynchronous block data transfers. Address mode is the time when the address/data control line is high. Information placed on the address/data lines of the MULTICHANNEL bus as two successive 16-bit words is interpreted to select or deselect a device on the bus and address the specific resource on the device. Typically, these address mode transfers are only 2 word sequences. Figure 5 is a timing diagram of the handshake routine in address mode. The data mode is the time when the address/data control line is low. Valid data is placed on the address/data lines of the bus and can occur only after an address mode has been performed. Transfers during data mode are usually large quantities of either 8- or 16-bit data, and are passed to or from the addressed device until it is deselected. Figure 6 is a timing diagram of a data transfer sequence.

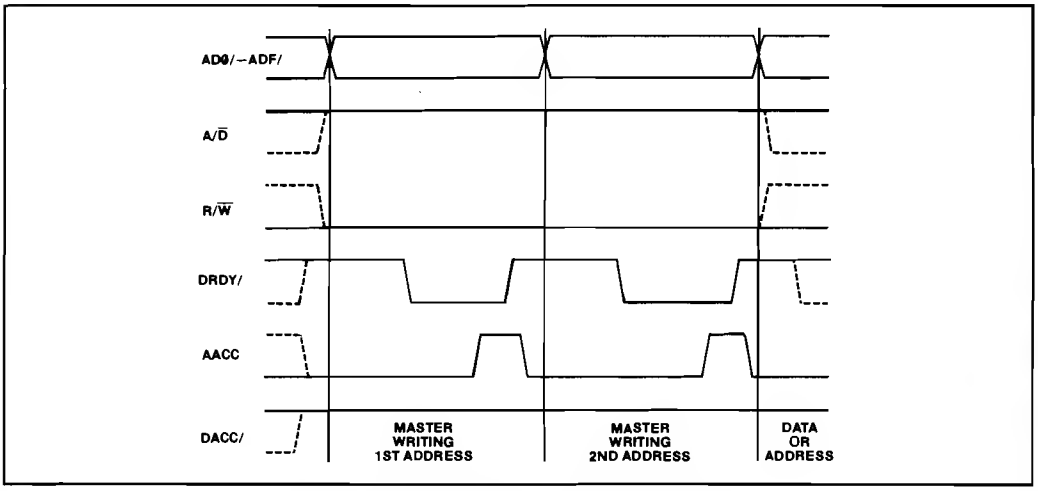

Figure 5. MULTICHANNEL™ Bus Address Cycle

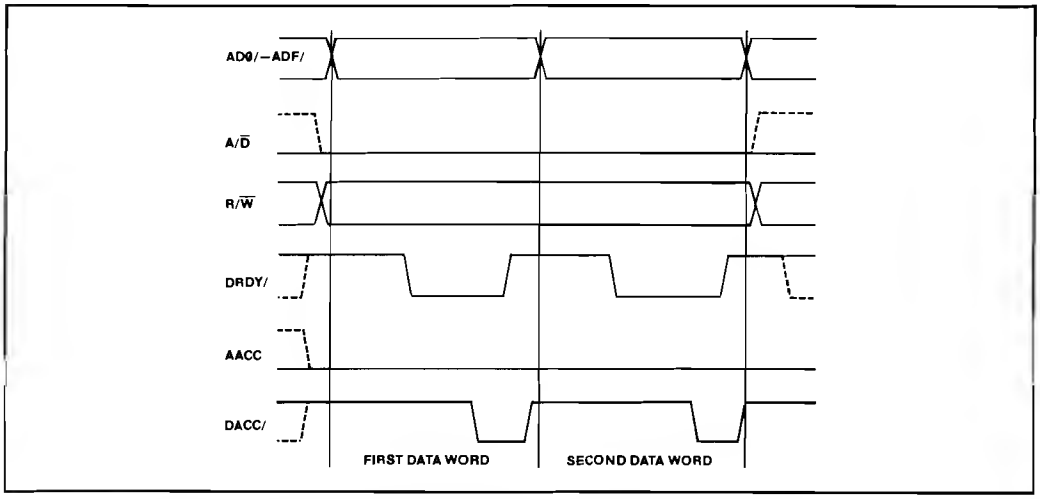

Figure 6. MULTICHANNEL™ Bus Data Transfer Sequence

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Control transfer mode is the time when the bus Supervisor selects the bus Controller and programs its registers with required information. Once programmed, a bus Controller may select a device and originate a data transfer operation.

The operational sequences of these transfer modes are similar in handling read and write operations to and from the 16 megabytes of memory and the 16 megabytes of registers addressable on each MULTICHANNEL device.

A typical transfer sequence begins when the master sends a two-word address sequence to select a MULTICHANNEL device and specify address, direction and resource (memory vs. I/O) of the data transfer. Following device selection, the Talker proceeds to send the data as a continuous 8 or 16-bit data word stream until the block data move is complete. The master terminates the transfer by issuing another two-word address sequence for device deselection.

The transfer sequence described is identical for both memory and register type transfers. The master controls similar read and write operations between devices, and the address select and deselect sequences use the same address format. Figure 7 contains the MULTICHANNEL bus address format.

DEVICE REGISTER DEFINITION

Of the 16 megabytes of register space per device, the first 16 registers are pre-defined to provide a standard register area common to all devices. The remaining registers are user definable. Table 2 lists the 16 defined registers along with their function. The use of this register concept allows for standard interface between all MULTICHANNEL devices. Please refer to the MULTICHANNEL Bus Specification for more detailed information.

Table 2. MULTICHANNEL™ Device Register Definitions

Register Number	Definition	Mode
0	STO/ Flag/Status	Read Only
1	SRQ/ Flag/Status	Read Only
2	SRQ/ Mask	Write Only
3	Device Command	Write Only
4	Device Parameter	Write Only
5	Data Address 1	Read or Write
6	Data Address 2	Read or Write
7	Block Length 1	Read or Write
8	Block Length 2	Read or Write
9	Error Address 1	Read Only
10	Error Address 2	Read Only
11	Address Extension	Write Only
12-15	Reserved	
16-16 Mbyte	User Defined	Read or Write

BUS INTERRUPT HANDLING

The MULTICHANNEL bus Supervisor, being responsible for bus access and control, monitors the two bus interrupt lines. The Supervisor Take-Over interrupt (STO) is used to inform the bus Supervisor that a device wants to return control of the bus to the Supervisor or that an error has occurred. The Service Request Interrupt (SRQ) is used by devices which do not have control of the bus, but require service from the bus Supervisor. To locate a device transmitting a bus interrupt, the bus Supervisor

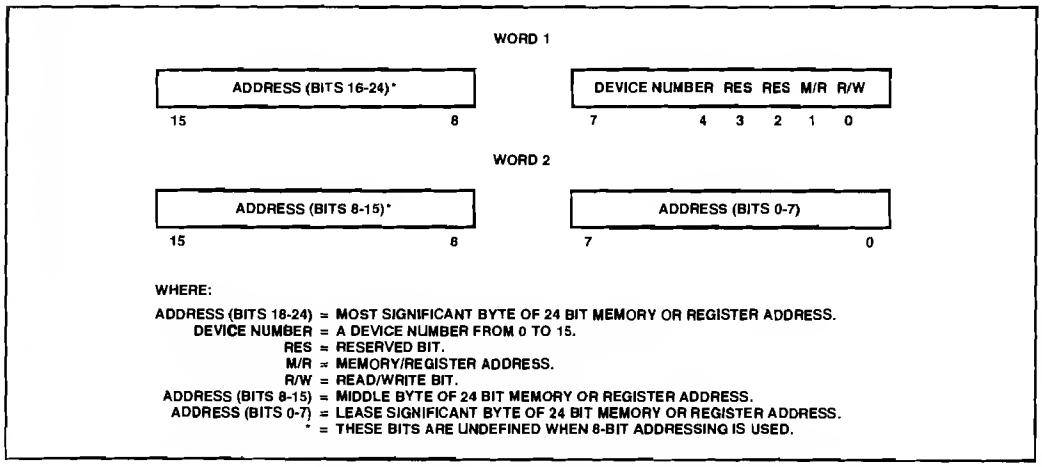

Figure 7. MULTICHANNEL™ Bus Address Format

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polls each device attached to the bus by reading the appropriate register of each device and testing for a non-zero value. In current implementations, the Supervisor polls each device only once. If the interrupt is not removed an error occurs.

PARITY AND RESET

Parity operation on the MULTICHANNEL bus is provided, but is not required. The bus Supervisor selects between parity mode and non-parity mode depending upon system requirements. If parity mode is selected all Talkers must generate odd parity. All active Listeners monitor the parity line and generate an STO interrupt signal if there is a parity error.

A reset function is also supported by the MULTICHANNEL bus, and is controlled by the bus Supervisor to bring the bus to a known state. It is used to reset all devices after power-up, and when required to gain control of the bus.

SPECIFICATIONS

Word Size

Data — 8, 16-bit

Memory Addressing

24-bits — 16 megabyte – direct access – automatic incrementing

Register Addressing

24-bits — 16 megabyte – direct access

Electrical Characteristics

DC SPECIFICATIONS

Maximum Bus Length

15 meters (50 feet)

Bus Devices Supported

16 total devices — (Supervisor, Controller, and Talker/Listener)

Bus Bandwidth

8 megabytes/sec. — 16-bit

4 megabytes/sec. — 8-bit

Table 3. DC Specifications

Signal Name	Driver Type	Termination (see Note)	Min. Driver Requirements			Max. Receiver Requirements		
			High	Low	Load Cap	High	Low	Load Cap
AD15-0/	TRI-STATE	110 Ohms	– 5 ma	48 ma	300 pf	0.2 ma	0.8 ma	15 pf
SA/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
RESET/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
AACC	OPEN COLL	1K/2K Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
DACC/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
SRQ/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
STO/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
R/W	DIF, NON-INV	220/470 Ohms	– 20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
R/W/	DIF, INV	470/220 Ohms	– 20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
A/D	DIF, NON-INV	220/470 Ohms	– 20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
A/D/	DIF, INV	470/220 Ohms	– 20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
PB/	DIF, NON-INV	220/470 Ohms	– 20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
PB*/	DIF, INV	470/220 Ohms	– 20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
DRDY/	DIF, NON-INV	220/470 Ohms	– 20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
DRDY*/	DIF, INV	470/220 Ohms	– 20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.

NOTE: Termination provided only at the physically ends of the interconnect cable. Where the positive termination (pull-up) resistance is different from the negative termination (pull-down) resistance, the positive termination resistance is listed first.

BUS TIMING

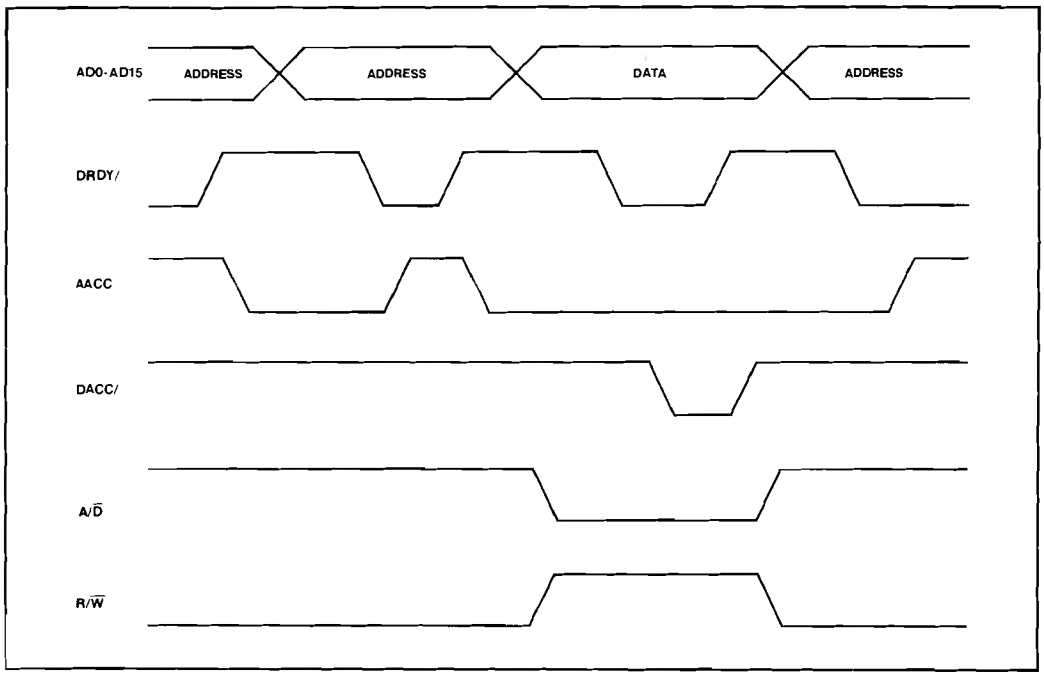


Figure 8. Address-Read-Address-Write Cycles

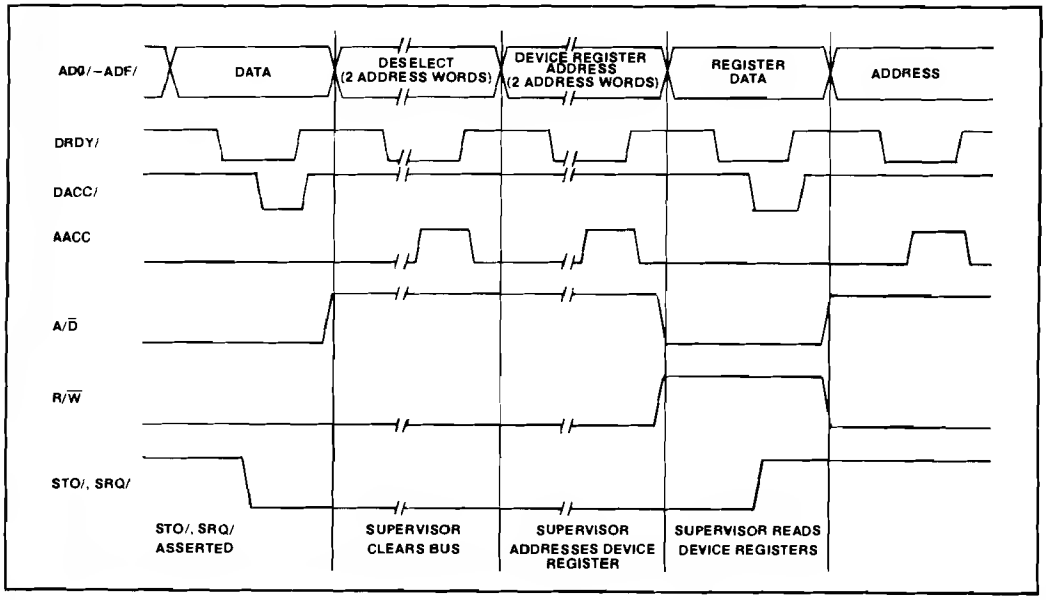


Figure 9. Supervisor Interrupt Timing

Cables and Connectors

Table 3. Cable and Receptacle Vendors

MULTICHANNEL™ Bus Compatible Cable			
Vendor	**Ribbon Type**	**Vendor No.**	**Conductor**
Belden	Plain Flat	9L28060	60
Belden	Twisted-Pair	9V28060	60
Belden	Insulated Flat	9L28260	60
Spectrastrip	Plain Flat	455-240-60	60
Spectrastrip	Twisted-Pair	455-248-60	60
Spectrastrip	Insulated Flat	151-2830-060	60
MULTICHANNEL™ Bus Compatible Receptacles			
Vendor	**Type**	**Vendor No.**	**Pins**
Berg	Male	65823-103	60
Berg	Female	65949-960	60
3M	Male	3372-1302	60
3M	Female	3334-6000	60

PHYSICAL PROPERTIES

Conductors — 28 AWG, 7/36 strand, tinned copper

Conductor Insulation — 0.010 inch wall, nominal

Conductor Spacing — Twisted pair – 0.10 inch, nominal; Flat – 0.050 inch, ±10%

Cable Thickness — Flat – 0.042 inch, nominal

Temperature Rating — 80°C

ELECTRICAL PROPERTIES

Impedance (nominal) — 105 ohms ±10%

Propagation Velocity (nominal) — 1.7 ns/ft

Capacitance (nominal) — 22 pf/ft

INSULATION REQUIREMENTS

Voltage Rating (minimum) — 100 Vdc

Insulation Resistance (minimum) — 1×10^{10} ohms

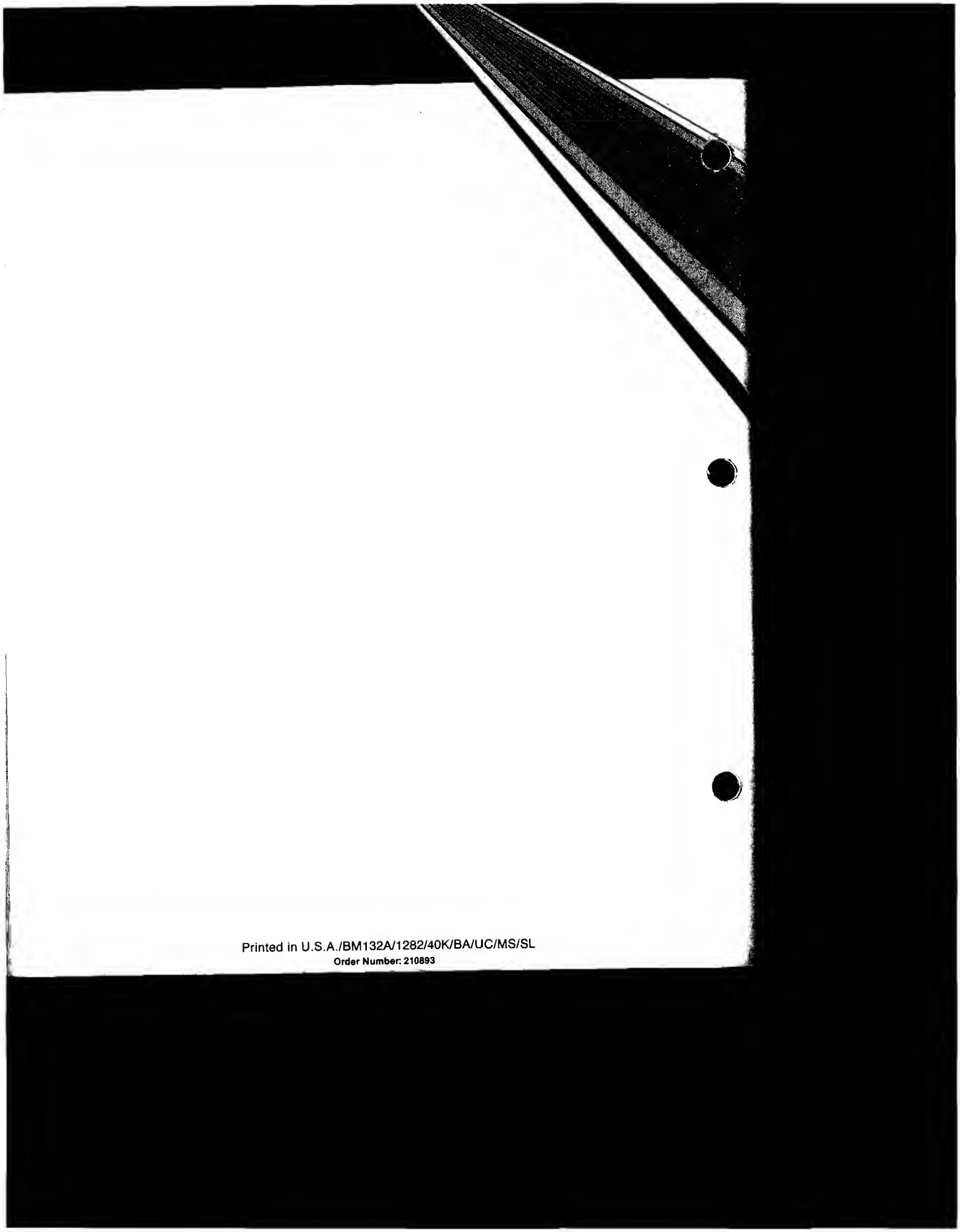
Environmental Characteristics

Temperature — 0 - 55°C

Humidity — 90% max. relative (no condensation)

Reference Manuals

210883 — MULTIBUS Architecture Handbook.



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